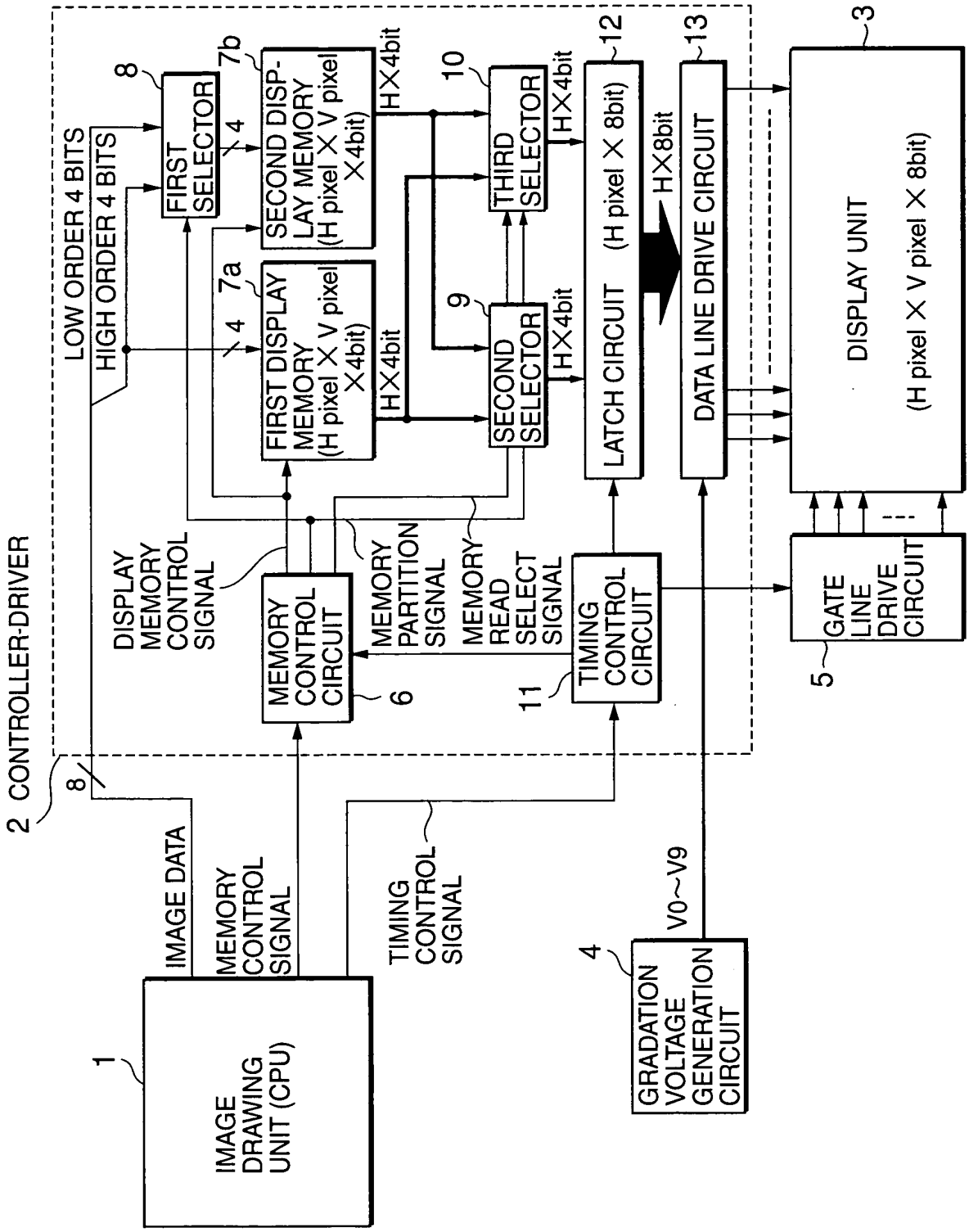
2 CONTROLLER-DRIVER
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
8
FIRST SELECTOR
4
7b
SECOND DISPLAY MEMORY (H pixel × V pixel ×4bit)
H×4bit
10
THIRD SELECTOR
H×4bit
12
LATCH CIRCUIT (H pixel × 8bit)
H×8bit
13
DATA LINE DRIVE CIRCUIT
3
DISPLAY UNIT (H pixel × V pixel × 8bit)
4
7a
FIRST DISPLAY MEMORY (H pixel × V pixel ×4bit)
H×4bit
9
SECOND SELECTOR
H×4bit
DISPLAY MEMORY CONTROL SIGNAL
MEMORY CONTROL CIRCUIT
6
MEMORY PARTITION SIGNAL
MEMORY READ SELECT SIGNAL
11
TIMING CONTROL CIRCUIT
GATE LINE DRIVE CIRCUIT
5
8
IMAGE DATA
MEMORY CONTROL SIGNAL
TIMING CONTROL SIGNAL
1
IMAGE DRAWING UNIT (CPU)
4
V0～V9
GRADATION VOLTAGE GENERATION CIRCUIT

FIG. 1

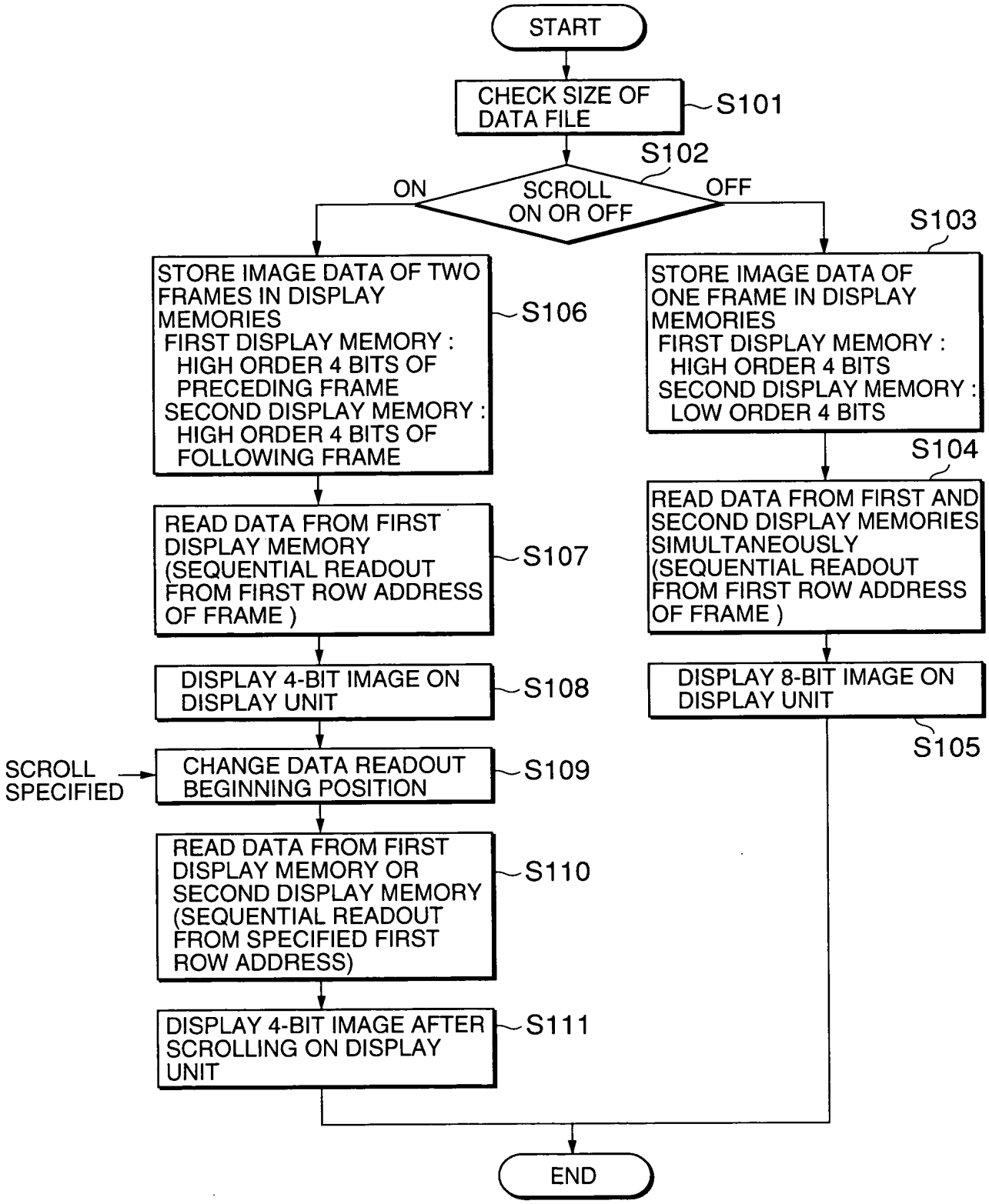
START
CHECK SIZE OF DATA FILE
S101
S102
SCROLL ON OR OFF
ON
OFF
S103
STORE IMAGE DATA OF TWO FRAMES IN DISPLAY MEMORIES
FIRST DISPLAY MEMORY : HIGH ORDER 4 BITS OF PRECEDING FRAME
SECOND DISPLAY MEMORY : HIGH ORDER 4 BITS OF FOLLOWING FRAME
S106
STORE IMAGE DATA OF ONE FRAME IN DISPLAY MEMORIES
FIRST DISPLAY MEMORY : HIGH ORDER 4 BITS
SECOND DISPLAY MEMORY : LOW ORDER 4 BITS
S104
READ DATA FROM FIRST DISPLAY MEMORY (SEQUENTIAL READOUT FROM FIRST ROW ADDRESS OF FRAME)
S107
READ DATA FROM FIRST AND SECOND DISPLAY MEMORIES SIMULTANEOUSLY (SEQUENTIAL READOUT FROM FIRST ROW ADDRESS OF FRAME)
DISPLAY 4-BIT IMAGE ON DISPLAY UNIT
S108
DISPLAY 8-BIT IMAGE ON DISPLAY UNIT
S105
SCROLL SPECIFIED
CHANGE DATA READOUT BEGINNING POSITION
S109
READ DATA FROM FIRST DISPLAY MEMORY OR SECOND DISPLAY MEMORY (SEQUENTIAL READOUT FROM SPECIFIED FIRST ROW ADDRESS)
S110
DISPLAY 4-BIT IMAGE AFTER SCROLLING ON DISPLAY UNIT
S111
END

FIG. 2

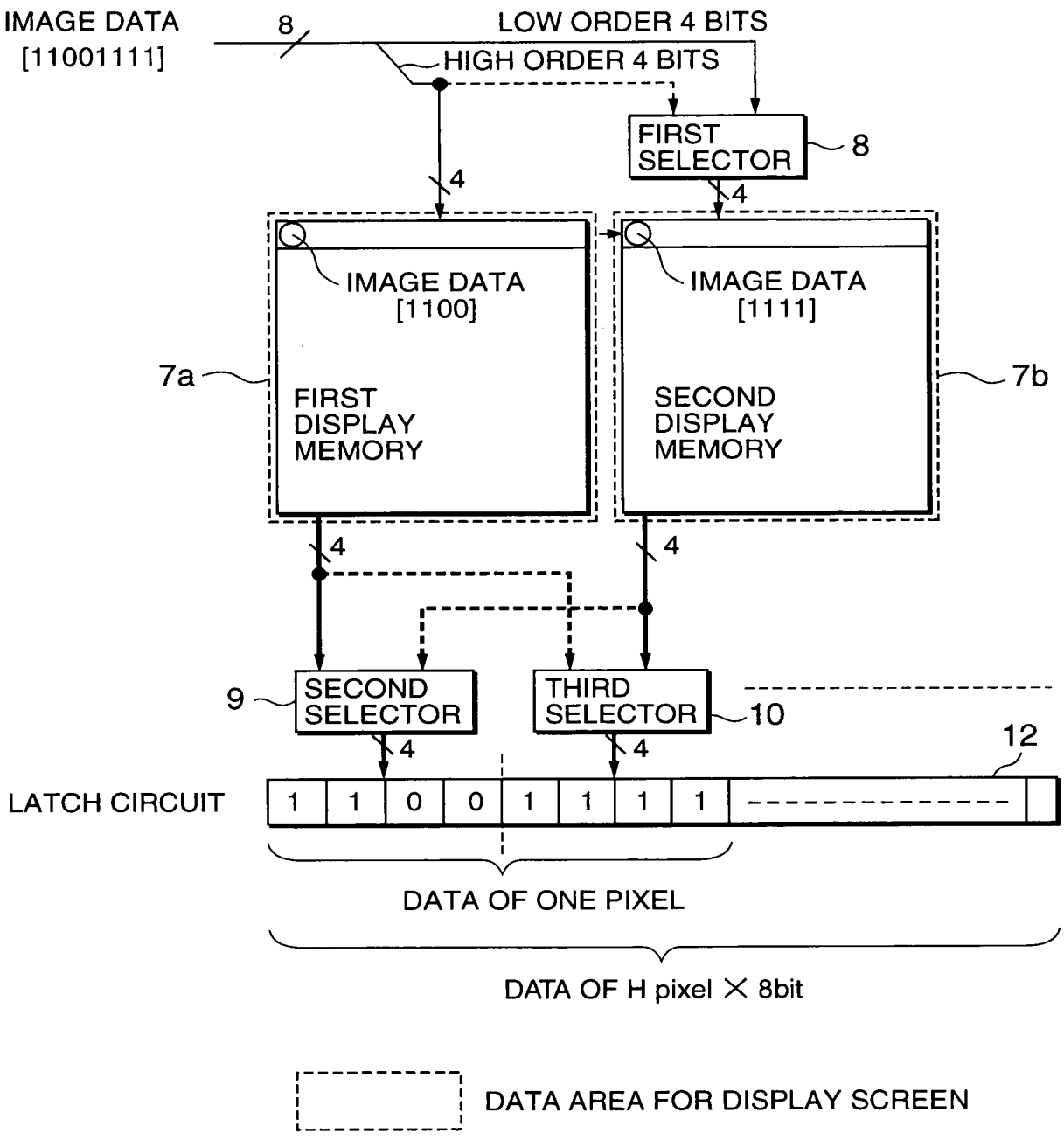
IMAGE DATA
[11001111]
8
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
FIRST SELECTOR
8
4
4
IMAGE DATA
[1100]
IMAGE DATA
[1111]
7a
FIRST DISPLAY MEMORY
SECOND DISPLAY MEMORY
7b
4
4
9
SECOND SELECTOR
THIRD SELECTOR
10
12
4
4
LATCH CIRCUIT
1 1 0 0 1 1 1 1
DATA OF ONE PIXEL
DATA OF H pixel × 8bit
DATA AREA FOR DISPLAY SCREEN

FIG. 3

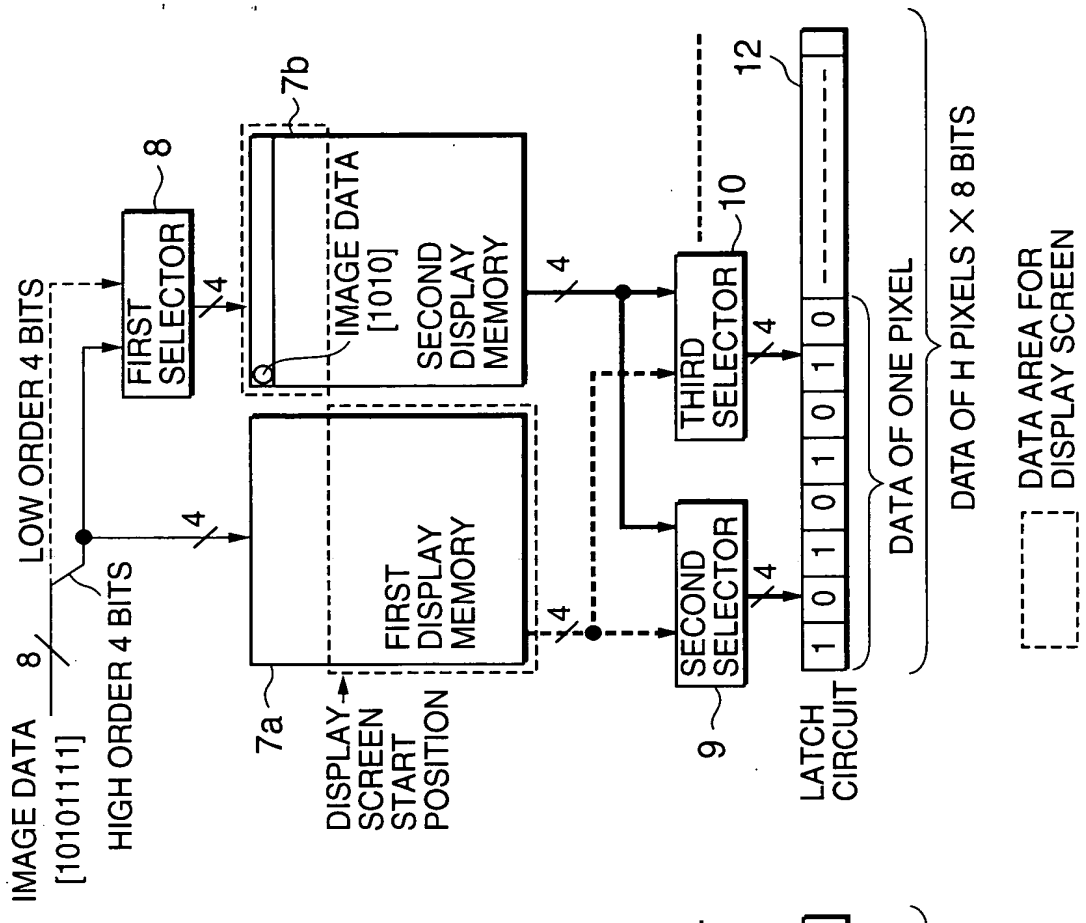
IMAGE DATA [10101111]
8
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
FIRST SELECTOR
8
4
7b
IMAGE DATA [1010]
SECOND DISPLAY MEMORY
4
FIRST DISPLAY MEMORY
7a
DISPLAY SCREEN START POSITION
4
THIRD SELECTOR
10
SECOND SELECTOR
9
12
1 0 1 0 1 0 1 0
LATCH CIRCUIT
DATA OF ONE PIXEL
DATA OF H PIXELS X 8 BITS
DATA AREA FOR DISPLAY SCREEN

FIG. 4B

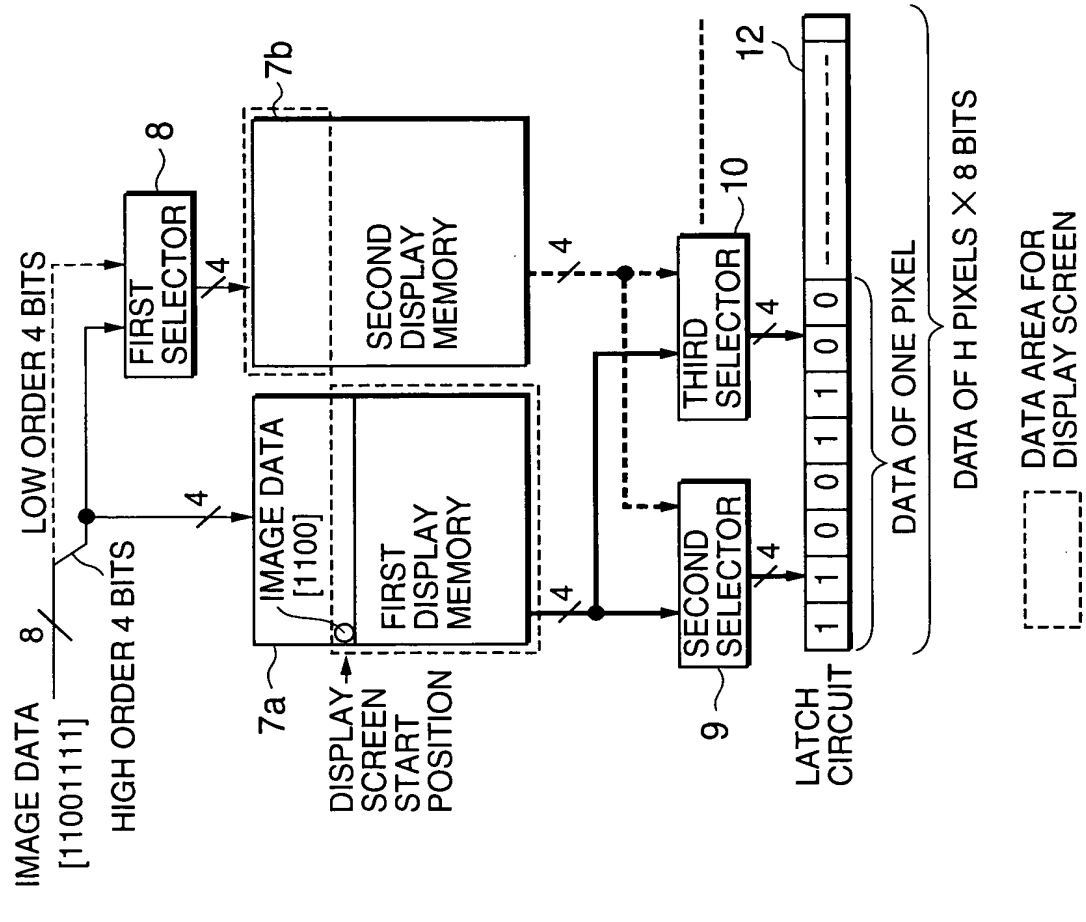
IMAGE DATA [11001111]
8
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
FIRST SELECTOR
8
4
7b
SECOND DISPLAY MEMORY
4
IMAGE DATA [1100]
FIRST DISPLAY MEMORY
7a
DISPLAY SCREEN START POSITION
4
THIRD SELECTOR
10
SECOND SELECTOR
9
12
1 1 0 0 1 1 0 0
LATCH CIRCUIT
DATA OF ONE PIXEL
DATA OF H PIXELS X 8 BITS
DATA AREA FOR DISPLAY SCREEN

FIG. 4A

MEMORY PARTITION SIGNAL (SELECT 1)	MEMORY READ SELECT SIGNAL (SELECT 2)	FIRST SELECTOR OUTPUT	SECOND SELECTOR OUTPUT	THIRD SELECTOR OUTPUT
OFF	OFF	LOW ORDER 4 BITS OF IMAGE DATA	— —	— —
OFF	ON	LOW ORDER 4 BITS OF IMAGE DATA	DATA STORED IN FIRST DISPLAY MEMORY	DATA STORED IN SECOND DISPLAY MEMORY
ON	OFF	HIGH ORDER 4 BITS OF IMAGE DATA	DATA STORED IN FIRST DISPLAY MEMORY	DATA STORED IN FIRST DISPLAY MEMORY
ON	ON	HIGH ORDER 4 BITS OF IMAGE DATA	DATA STORED IN SECOND DISPLAY MEMORY	DATA STORED IN SECOND DISPLAY MEMORY

FIG. 5

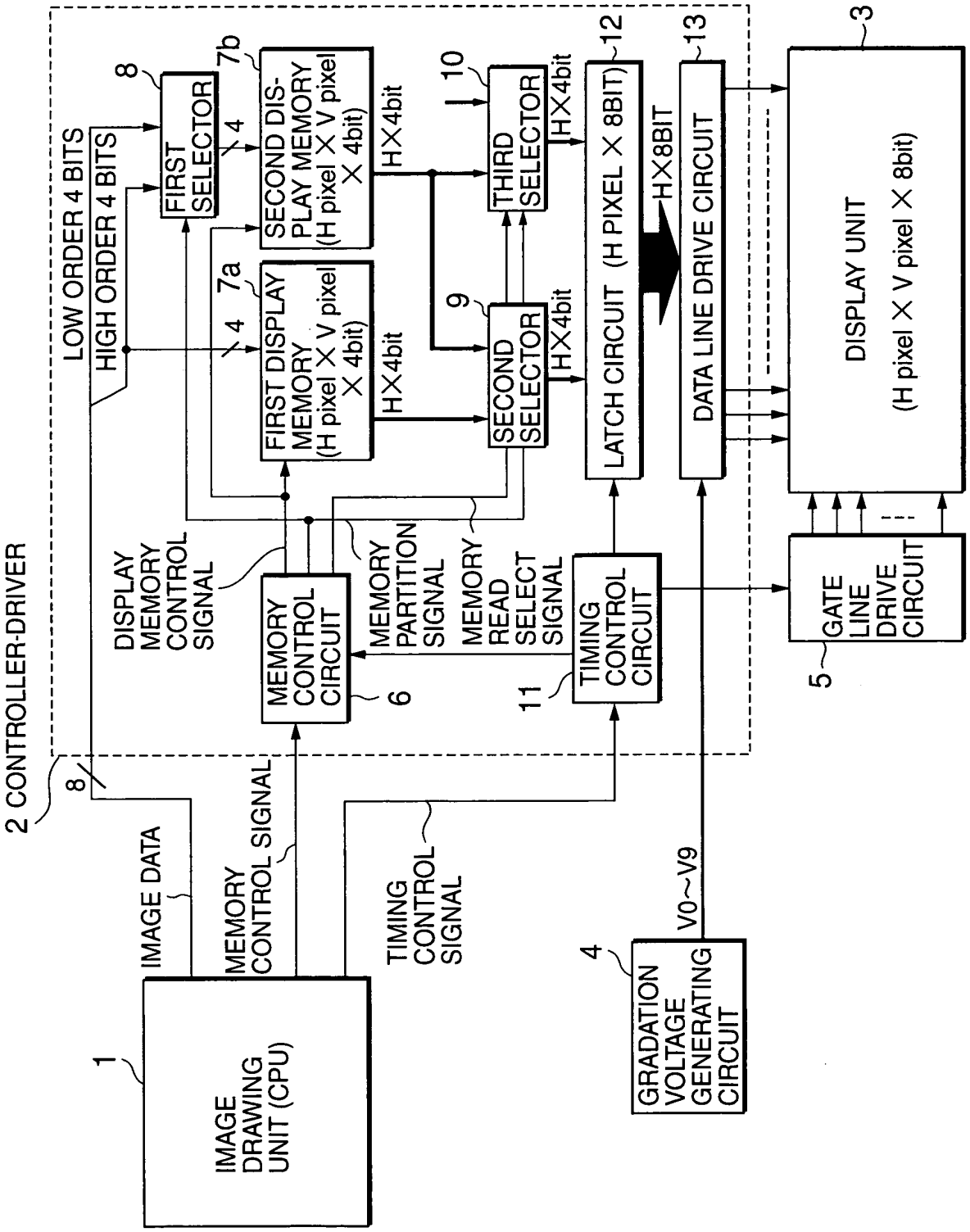
2 CONTROLLER-DRIVER
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
8
FIRST SELECTOR
4
7b
SECOND DISPLAY MEMORY (H pixel × V pixel × 4bit)
H×4bit
10
THIRD SELECTOR
H×4bit
12
LATCH CIRCUIT (H PIXEL × 8BIT)
13
H×8BIT
DATA LINE DRIVE CIRCUIT
3
DISPLAY UNIT
(H pixel × V pixel × 8bit)
4
7a
FIRST DISPLAY MEMORY (H pixel × V pixel × 4bit)
H×4bit
9
SECOND SELECTOR
H×4bit
DISPLAY MEMORY CONTROL SIGNAL
MEMORY CONTROL CIRCUIT
6
MEMORY PARTITION SIGNAL
MEMORY READ SELECT SIGNAL
11
TIMING CONTROL CIRCUIT
GATE LINE DRIVE CIRCUIT
5
8
IMAGE DATA
MEMORY CONTROL SIGNAL
TIMING CONTROL SIGNAL
V0~V9
4
GRADATION VOLTAGE GENERATING CIRCUIT
1
IMAGE DRAWING UNIT (CPU)

FIG. 6

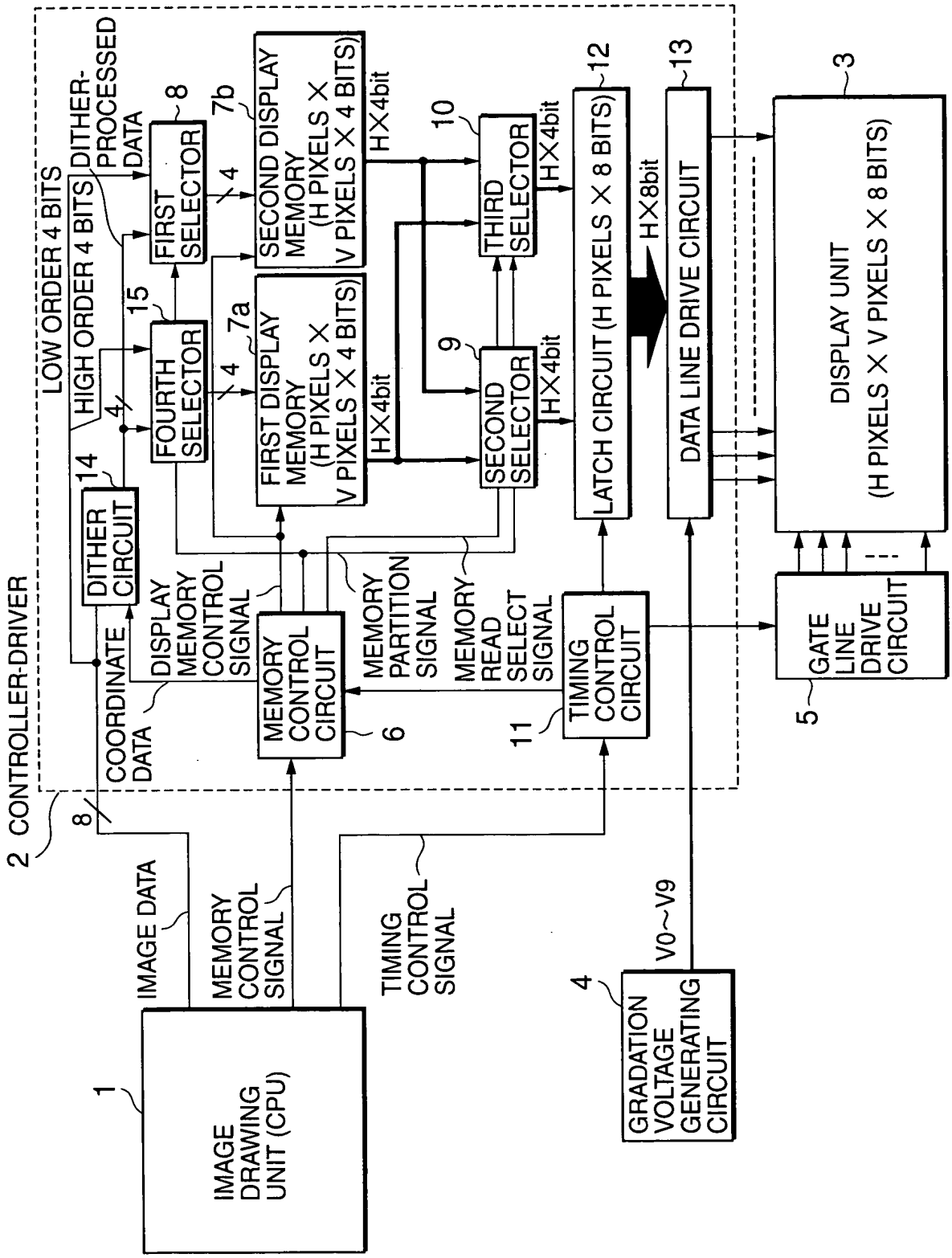
2 CONTROLLER-DRIVER
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
DITHER-PROCESSED DATA
8
FIRST SELECTOR
7b
SECOND DISPLAY MEMORY (H PIXELS X V PIXELS X 4 BITS)
HX4bit
10
THIRD SELECTOR
HX4bit
12
LATCH CIRCUIT (H PIXELS X 8 BITS)
HX8bit
13
DATA LINE DRIVE CIRCUIT
3
DISPLAY UNIT (H PIXELS X V PIXELS X 8 BITS)
15
FOURTH SELECTOR
7a
FIRST DISPLAY MEMORY (H PIXELS X V PIXELS X 4 BITS)
HX4bit
9
SECOND SELECTOR
HX4bit
14
DITHER CIRCUIT
DISPLAY MEMORY CONTROL SIGNAL
MEMORY PARTITION SIGNAL
MEMORY READ SELECT SIGNAL
MEMORY CONTROL CIRCUIT
6
TIMING CONTROL CIRCUIT
11
GATE LINE DRIVE CIRCUIT
5
COORDINATE DATA
8
IMAGE DATA
MEMORY CONTROL SIGNAL
TIMING CONTROL SIGNAL
V0~V9
4
GRADATION VOLTAGE GENERATING CIRCUIT
1
IMAGE DRAWING UNIT (CPU)

FIG. 7

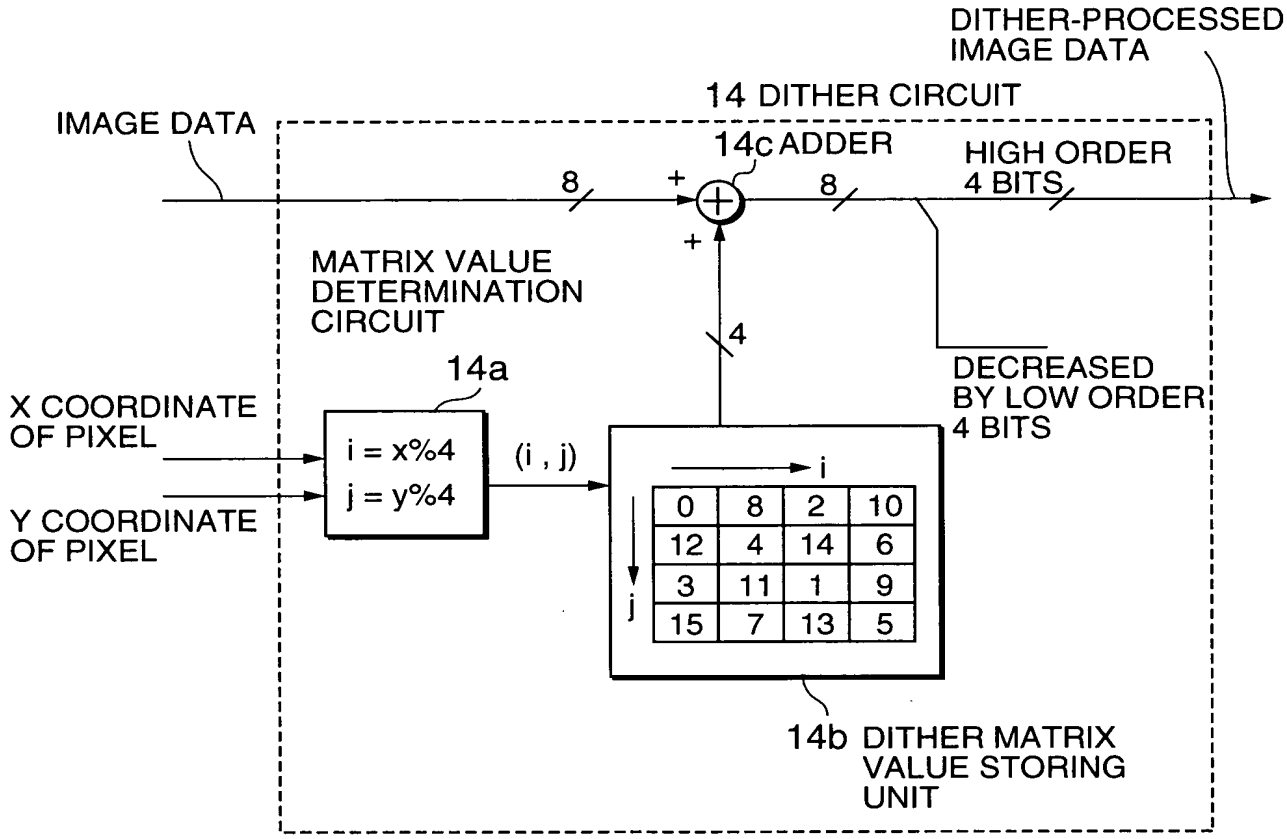
DITHER-PROCESSED IMAGE DATA
14 DITHER CIRCUIT
IMAGE DATA
14c ADDER
HIGH ORDER 4 BITS
8
+
8
+
MATRIX VALUE DETERMINATION CIRCUIT
4
14a
DECREASED BY LOW ORDER 4 BITS
X COORDINATE OF PIXEL
i = x%4
(i , j)
Y COORDINATE OF PIXEL
j = y%4
i
j
0 8 2 10
12 4 14 6
3 11 1 9
15 7 13 5
14b DITHER MATRIX VALUE STORING UNIT

FIG. 8

MEMORY PARTITION SIGNAL (SELECT 1)	MEMORY READ SELECT SIGNAL (SELECT 2)	FIRST SELECTOR OUTPUT	SECOND SELECTOR OUTPUT	THIRD SELECTOR OUTPUT	FOURTH SELECTOR OUTPUT
OFF	OFF	LOW ORDER 4 BITS OF IMAGE DATA	— —	— —	HIGH ORDER 4 BITS OF IMAGE DATA
OFF	ON	LOW ORDER 4 BITS OF IMAGE DATA	DATA STORED IN FIRST DISPLAY MEMORY	DATA STORED IN SECOND DISPLAY MEMORY	HIGH ORDER 4 BITS OF IMAGE DATA
ON	OFF	DITHER-PROCESSED IMAGE DATA (HIGH ORDER 4 BITS)	DATA STORED IN FIRST DISPLAY MEMORY	DATA STORED IN FIRST DISPLAY MEMORY	DITHER PROCESSED IMAGE DATA (HIGH ORDER 4 BITS)
ON	ON	DITHER PROCESSED IMAGE DATA (HIGH ORDER 4 BITS)	DATA STORED IN SECOND DISPLAY MEMORY	DATA STORED IN SECOND DISPLAY MEMORY	DITHER-PROCESSED IMAGE DATA (HIGH ORDER 4 BITS)

FIG. 9

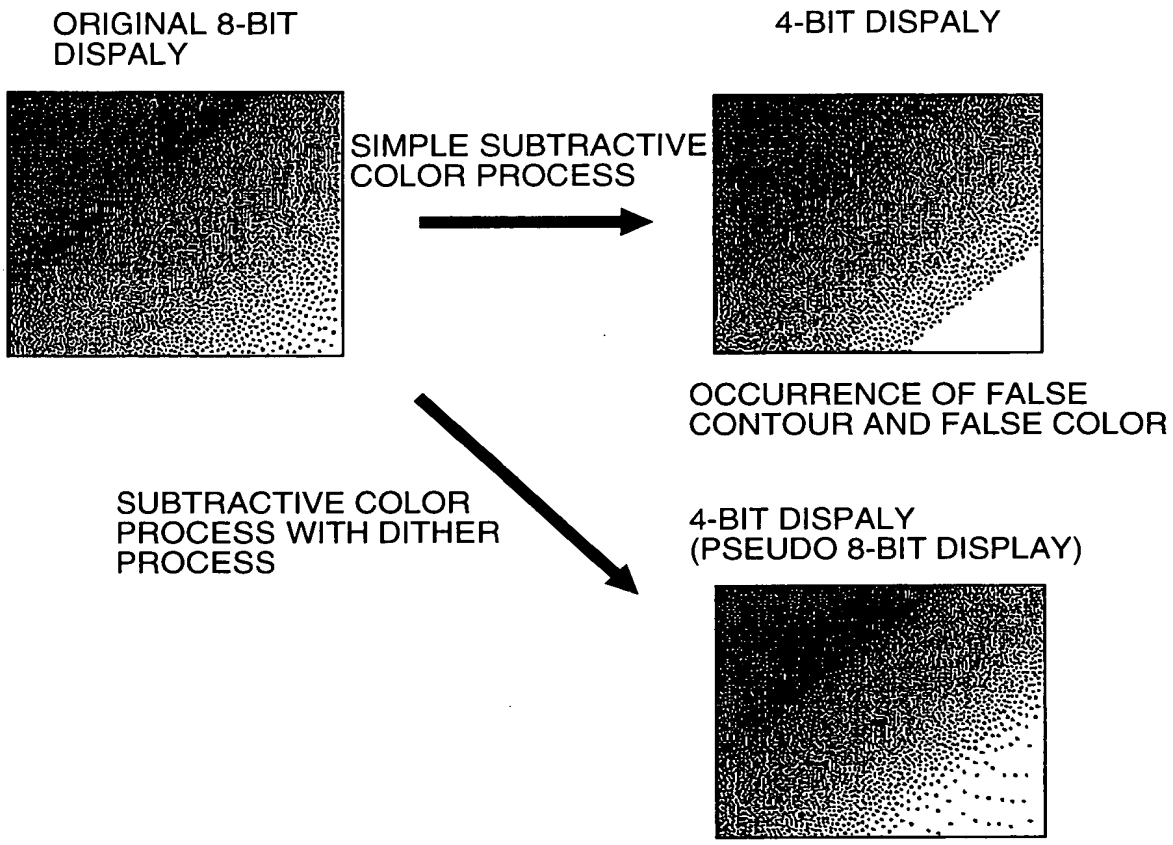
ORIGINAL 8-BIT DISPALY
4-BIT DISPALY
SIMPLE SUBTRACTIVE COLOR PROCESS
OCCURRENCE OF FALSE CONTOUR AND FALSE COLOR
SUBTRACTIVE COLOR PROCESS WITH DITHER PROCESS
4-BIT DISPALY (PSEUDO 8-BIT DISPLAY)

FIG. 10

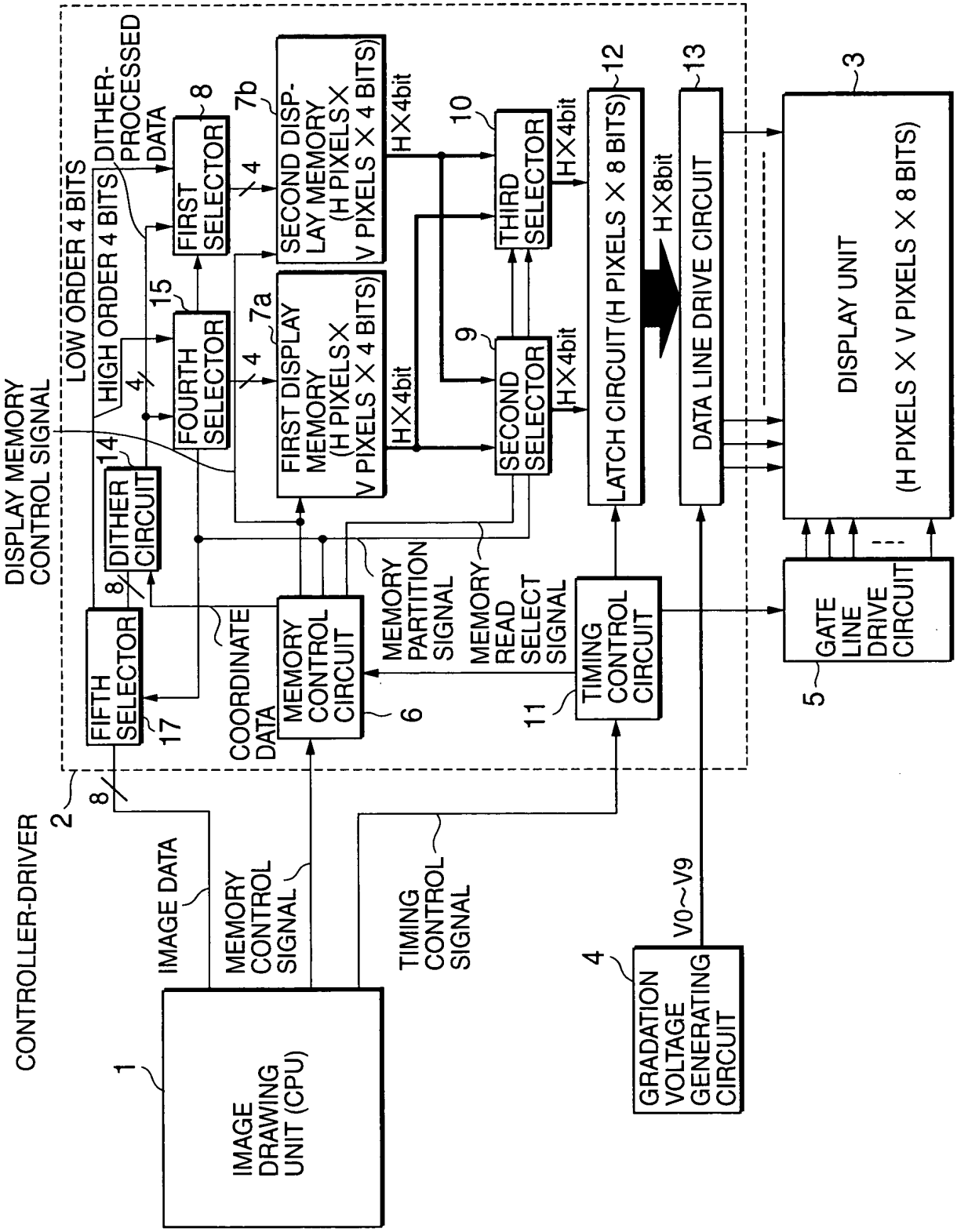
CONTROLLER-DRIVER
2
8
IMAGE DATA
MEMORY CONTROL SIGNAL
TIMING CONTROL SIGNAL
1
IMAGE DRAWING UNIT (CPU)
4
GRADATION VOLTAGE GENERATING CIRCUIT
V0~V9
DISPLAY MEMORY CONTROL SIGNAL
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
4
DITHER-PROCESSED DATA
8
FIRST SELECTOR
4
7b
SECOND DISPLAY MEMORY (H PIXELS X V PIXELS X 4 BITS)
HX4bit
10
THIRD SELECTOR
HX4bit
12
LATCH CIRCUIT (H PIXELS X 8 BITS)
HX8bit
13
DATA LINE DRIVE CIRCUIT
3
DISPLAY UNIT
(H PIXELS X V PIXELS X 8 BITS)
15
FOURTH SELECTOR
4
7a
FIRST DISPLAY MEMORY (H PIXELS X V PIXELS X 4 BITS)
HX4bit
9
SECOND SELECTOR
HX4bit
14
DITHER CIRCUIT
8
FIFTH SELECTOR
17
COORDINATE DATA
MEMORY CONTROL CIRCUIT
6
MEMORY PARTITION SIGNAL
MEMORY READ SELECT SIGNAL
11
TIMING CONTROL CIRCUIT
5
GATE LINE DRIVE CIRCUIT

FIG. 11

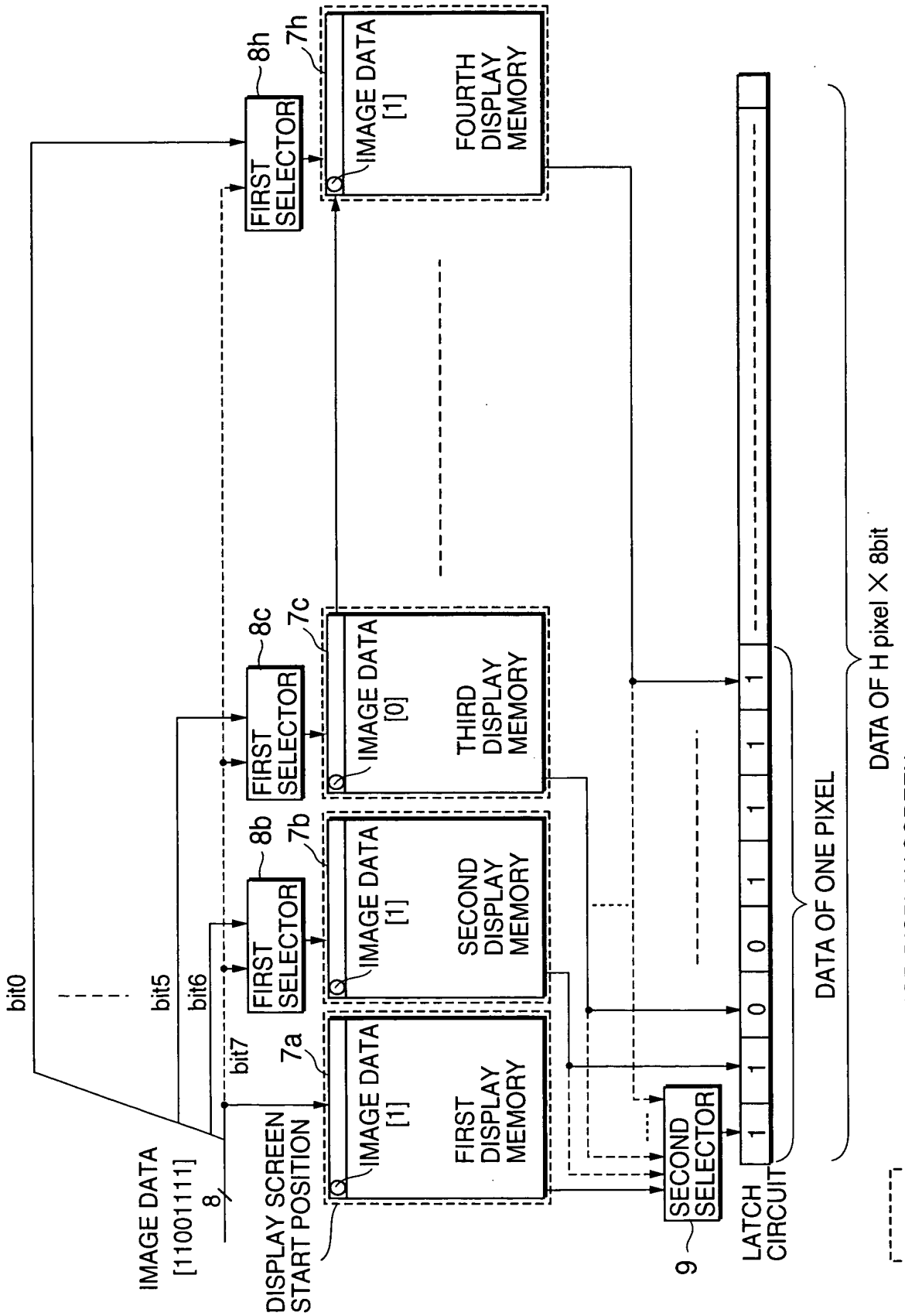
IMAGE DATA
[11001111]
8
DISPLAY SCREEN
START POSITION
bit0
bit5
bit6
bit7
FIRST SELECTOR
8b
8c
8h
7a
7b
7c
7h
IMAGE DATA
[1]
IMAGE DATA
[0]
FIRST DISPLAY MEMORY
SECOND DISPLAY MEMORY
THIRD DISPLAY MEMORY
FOURTH DISPLAY MEMORY
SECOND SELECTOR
9
LATCH CIRCUIT
1 1 0 0 1 1 1 1
DATA OF ONE PIXEL
DATA OF H pixel × 8bit
DATA AREA FOR DISPLAY SCREEN

FIG. 12

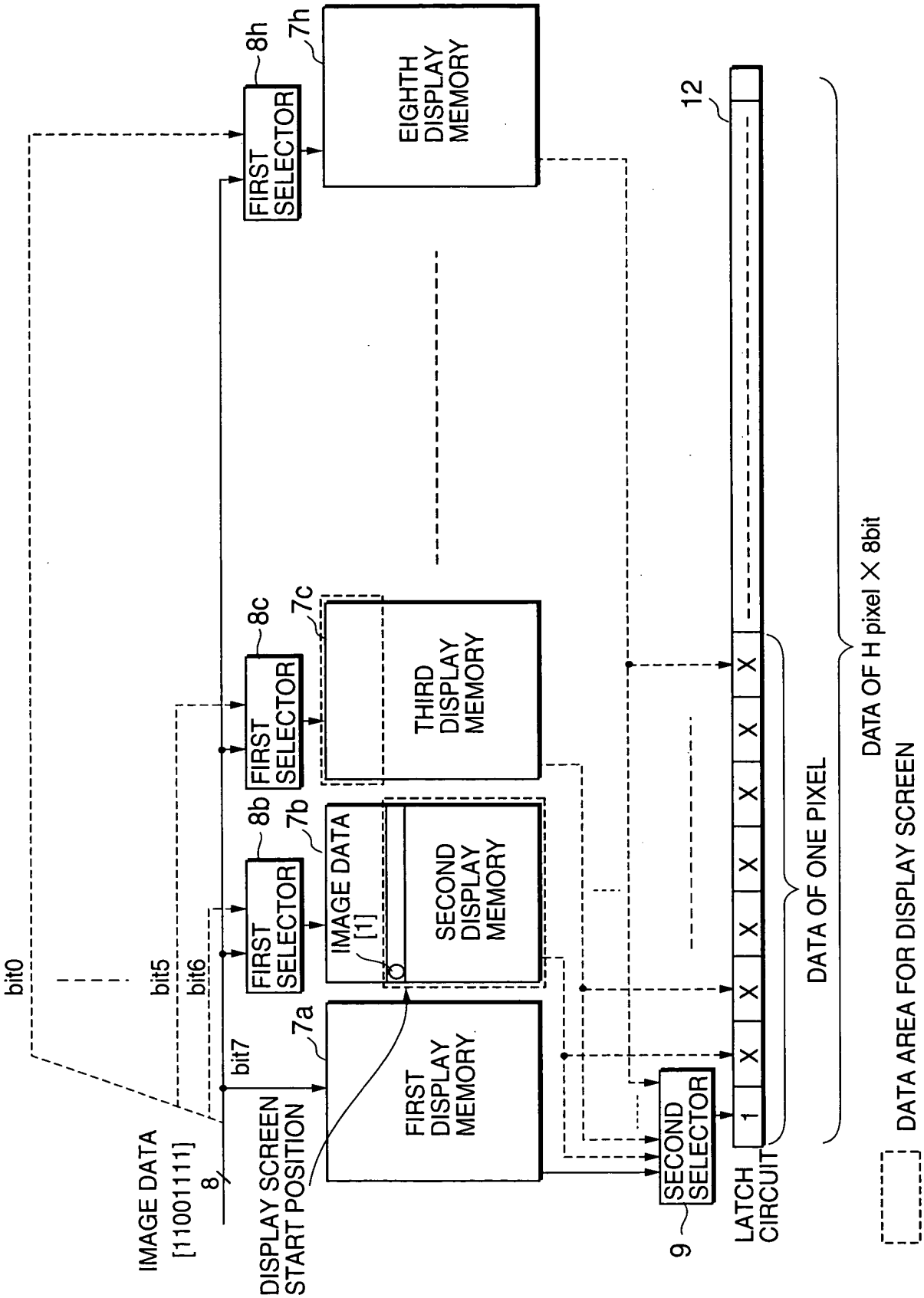
IMAGE DATA
[11001111]
8
DISPLAY SCREEN
START POSITION
bit0
bit5
bit6
bit7
FIRST
SELECTOR
8h
8c
8b
7h
7c
7b
7a
EIGHTH
DISPLAY
MEMORY
THIRD
DISPLAY
MEMORY
IMAGE DATA
[1]
SECOND
DISPLAY
MEMORY
FIRST
DISPLAY
MEMORY
SECOND
SELECTOR
9
12
LATCH
CIRCUIT
1
X
DATA OF ONE PIXEL
DATA OF H pixel X 8bit
DATA AREA FOR DISPLAY SCREEN

FIG. 13

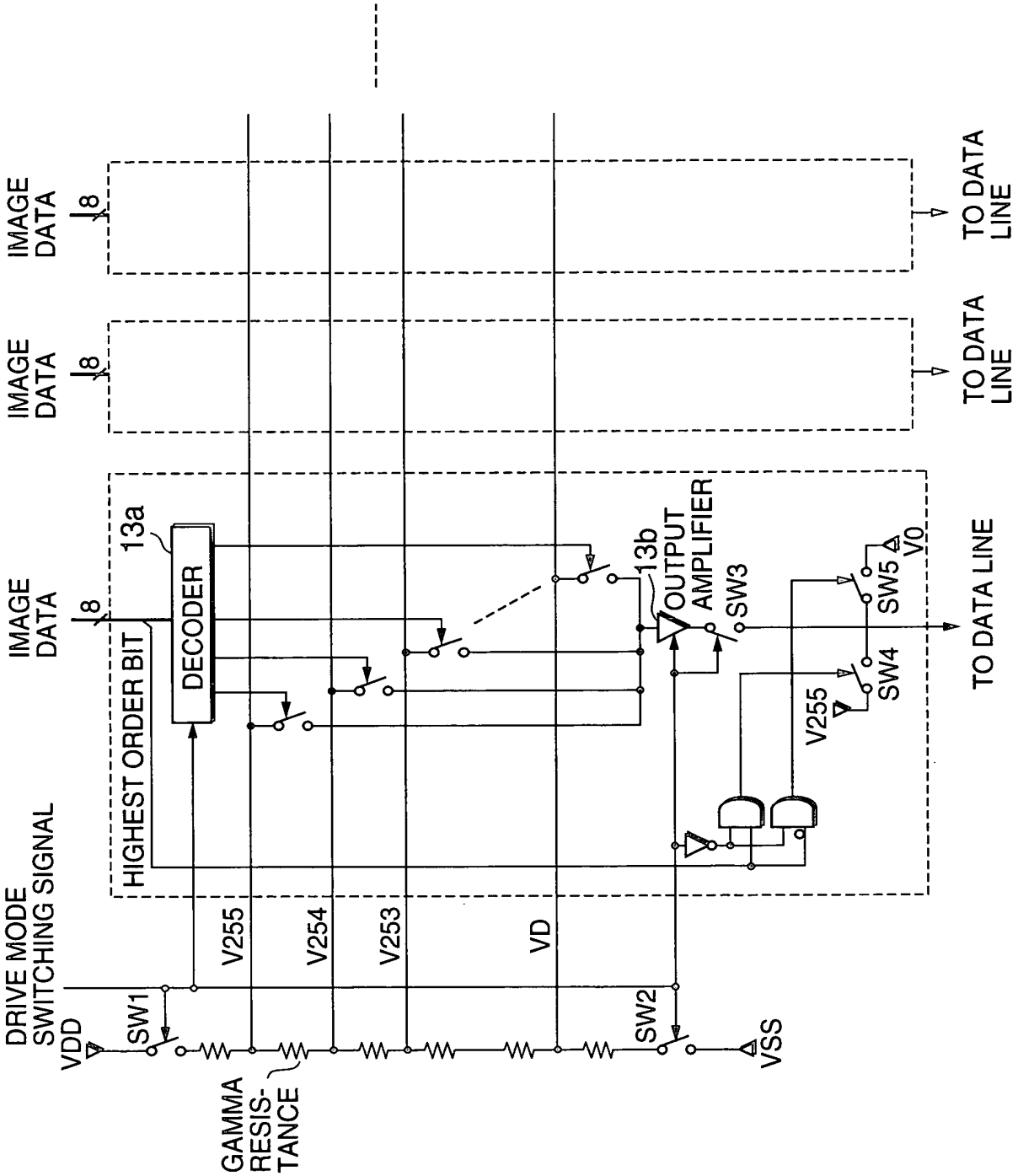
IMAGE DATA
8
TO DATA LINE
IMAGE DATA
8
TO DATA LINE
IMAGE DATA
8
13a
DECODER
HIGHEST ORDER BIT
13b
OUTPUT AMPLIFIER
SW3
SW5
V0
SW4
V255
TO DATA LINE
DRIVE MODE SWITCHING SIGNAL
VDD
SW1
V255
V254
V253
VD
SW2
VSS
GAMMA RESIS-TANCE

FIG. 14

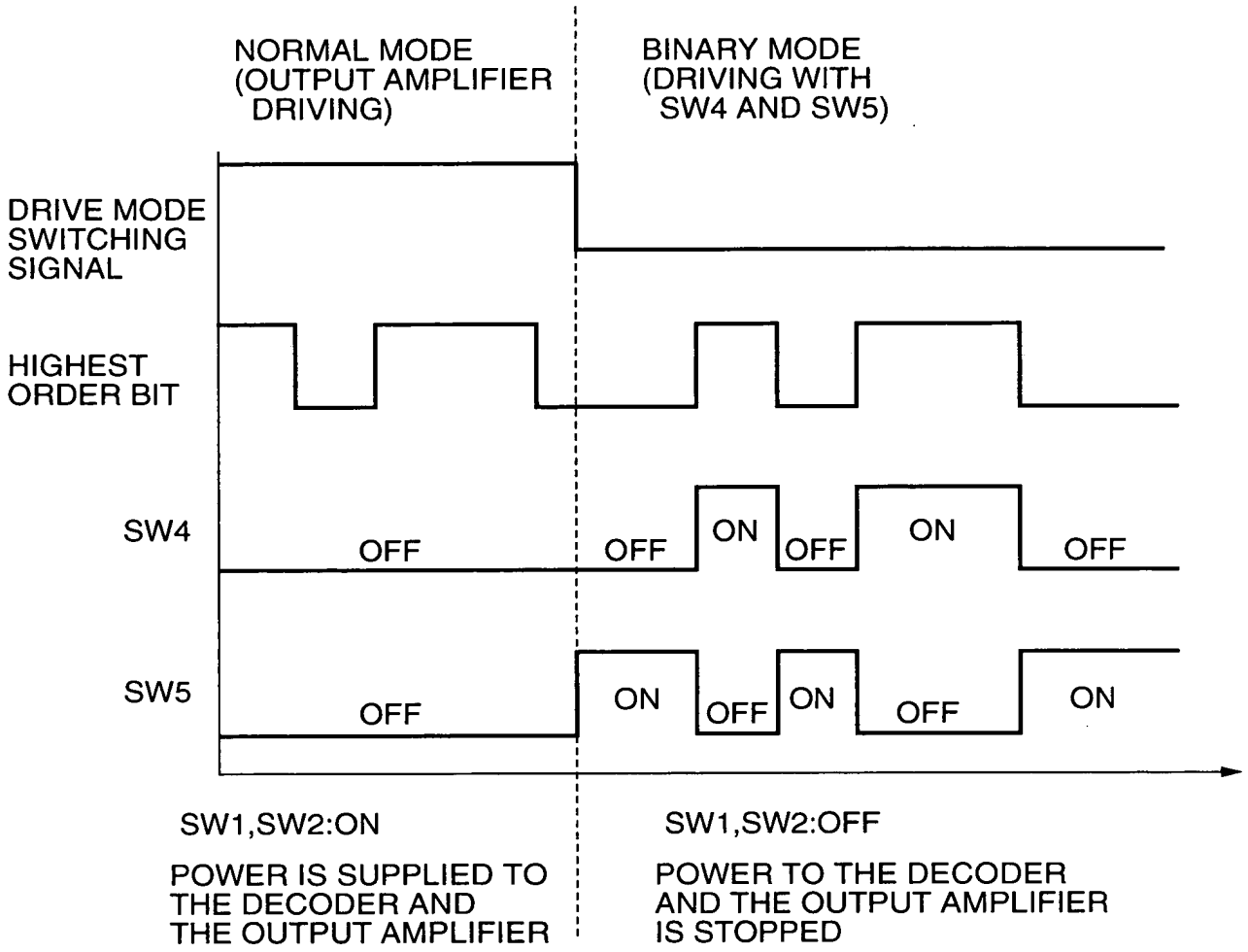
NORMAL MODE
(OUTPUT AMPLIFIER
DRIVING)
BINARY MODE
(DRIVING WITH
SW4 AND SW5)
DRIVE MODE
SWITCHING
SIGNAL
HIGHEST
ORDER BIT
SW4
OFF
OFF
ON
OFF
ON
OFF
SW5
OFF
ON
OFF
ON
OFF
ON
SW1,SW2:ON
POWER IS SUPPLIED TO
THE DECODER AND
THE OUTPUT AMPLIFIER
SW1,SW2:OFF
POWER TO THE DECODER
AND THE OUTPUT AMPLIFIER
IS STOPPED

FIG. 15

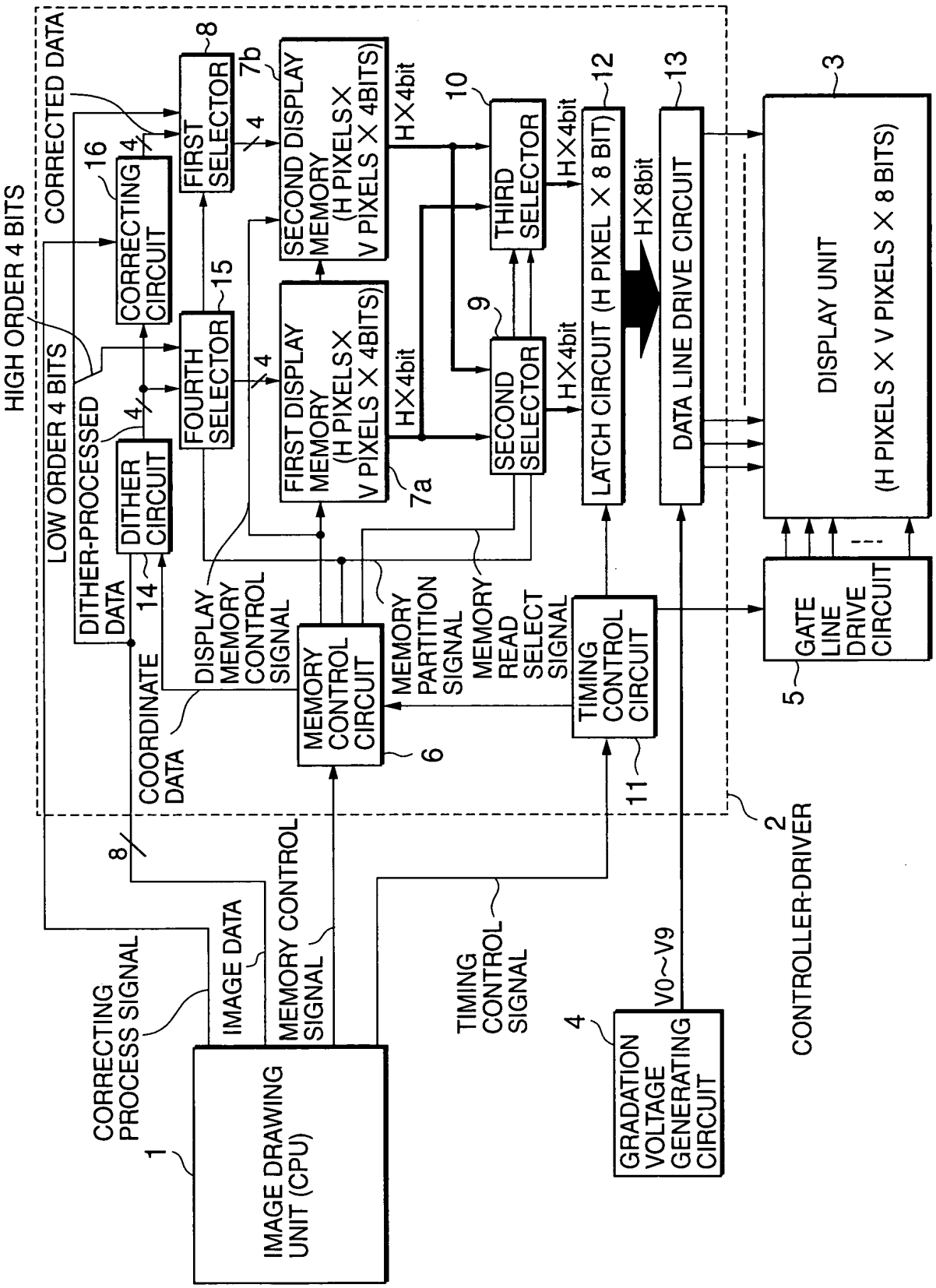
HIGH ORDER 4 BITS
LOW ORDER 4 BITS
CORRECTED DATA
DITHER-PROCESSED DATA
DITHER CIRCUIT
CORRECTING CIRCUIT
FIRST SELECTOR
FOURTH SELECTOR
FIRST DISPLAY MEMORY (H PIXELS× V PIXELS × 4BITS)
SECOND DISPLAY MEMORY (H PIXELS× V PIXELS × 4BITS)
HX4bit
THIRD SELECTOR
SECOND SELECTOR
LATCH CIRCUIT (H PIXEL × 8 BIT)
HX8bit
DATA LINE DRIVE CIRCUIT
DISPLAY UNIT
(H PIXELS × V PIXELS × 8 BITS)
GATE LINE DRIVE CIRCUIT
COORDINATE DATA
DISPLAY MEMORY CONTROL SIGNAL
MEMORY CONTROL CIRCUIT
MEMORY PARTITION SIGNAL
MEMORY READ SELECT SIGNAL
TIMING CONTROL CIRCUIT
CONTROLLER-DRIVER
CORRECTING PROCESS SIGNAL
IMAGE DATA
MEMORY CONTROL SIGNAL
TIMING CONTROL SIGNAL
V0~V9
GRADATION VOLTAGE GENERATING CIRCUIT
IMAGE DRAWING UNIT (CPU)

FIG. 16

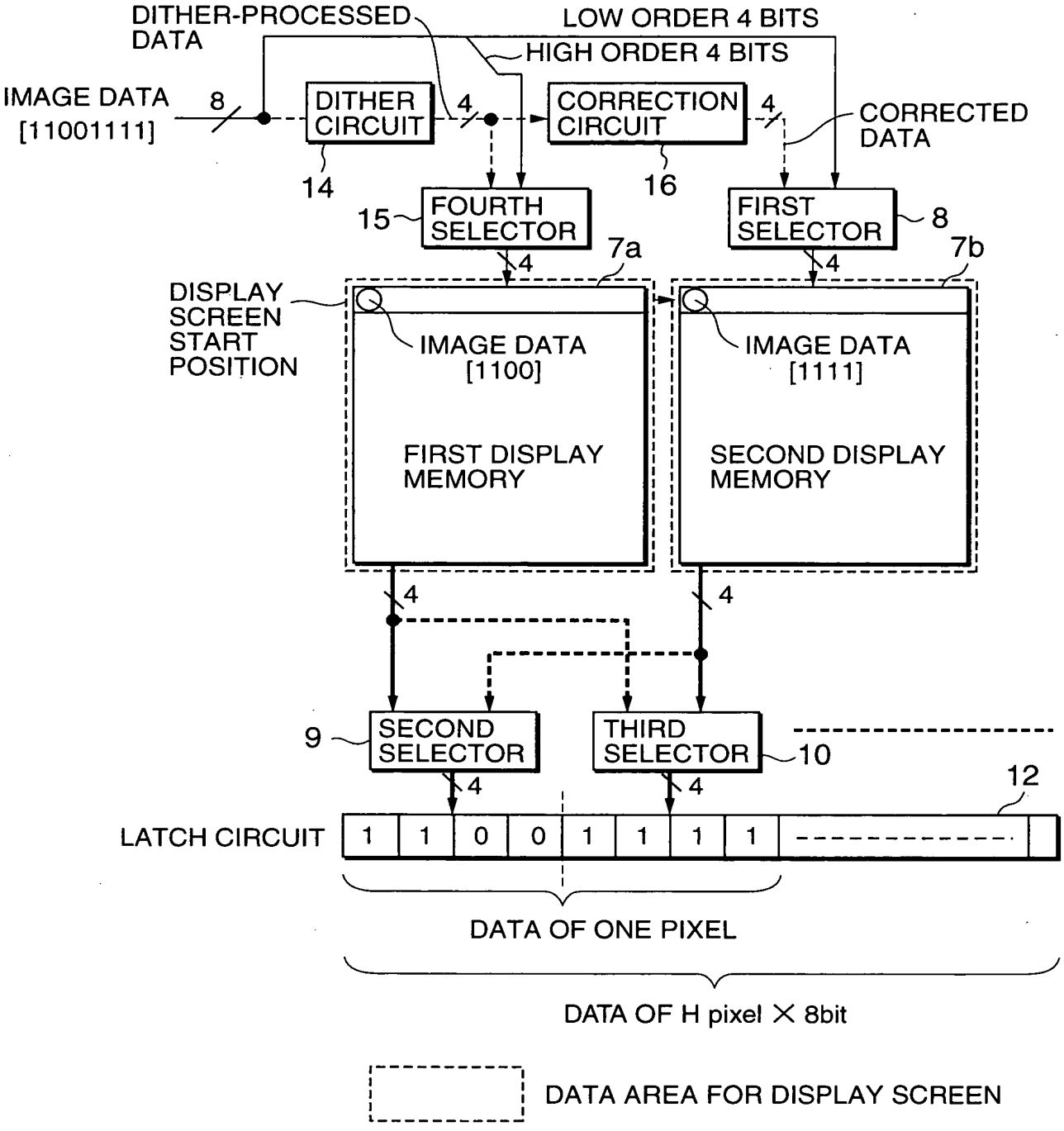
DITHER-PROCESSED DATA
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
IMAGE DATA [11001111]
8
DITHER CIRCUIT
4
CORRECTION CIRCUIT
4
CORRECTED DATA
14
16
15
FOURTH SELECTOR
FIRST SELECTOR
8
4
7a
7b
DISPLAY SCREEN START POSITION
IMAGE DATA [1100]
FIRST DISPLAY MEMORY
IMAGE DATA [1111]
SECOND DISPLAY MEMORY
9
SECOND SELECTOR
THIRD SELECTOR
10
12
LATCH CIRCUIT
1 1 0 0 1 1 1 1
DATA OF ONE PIXEL
DATA OF H pixel × 8bit
DATA AREA FOR DISPLAY SCREEN

FIG. 17

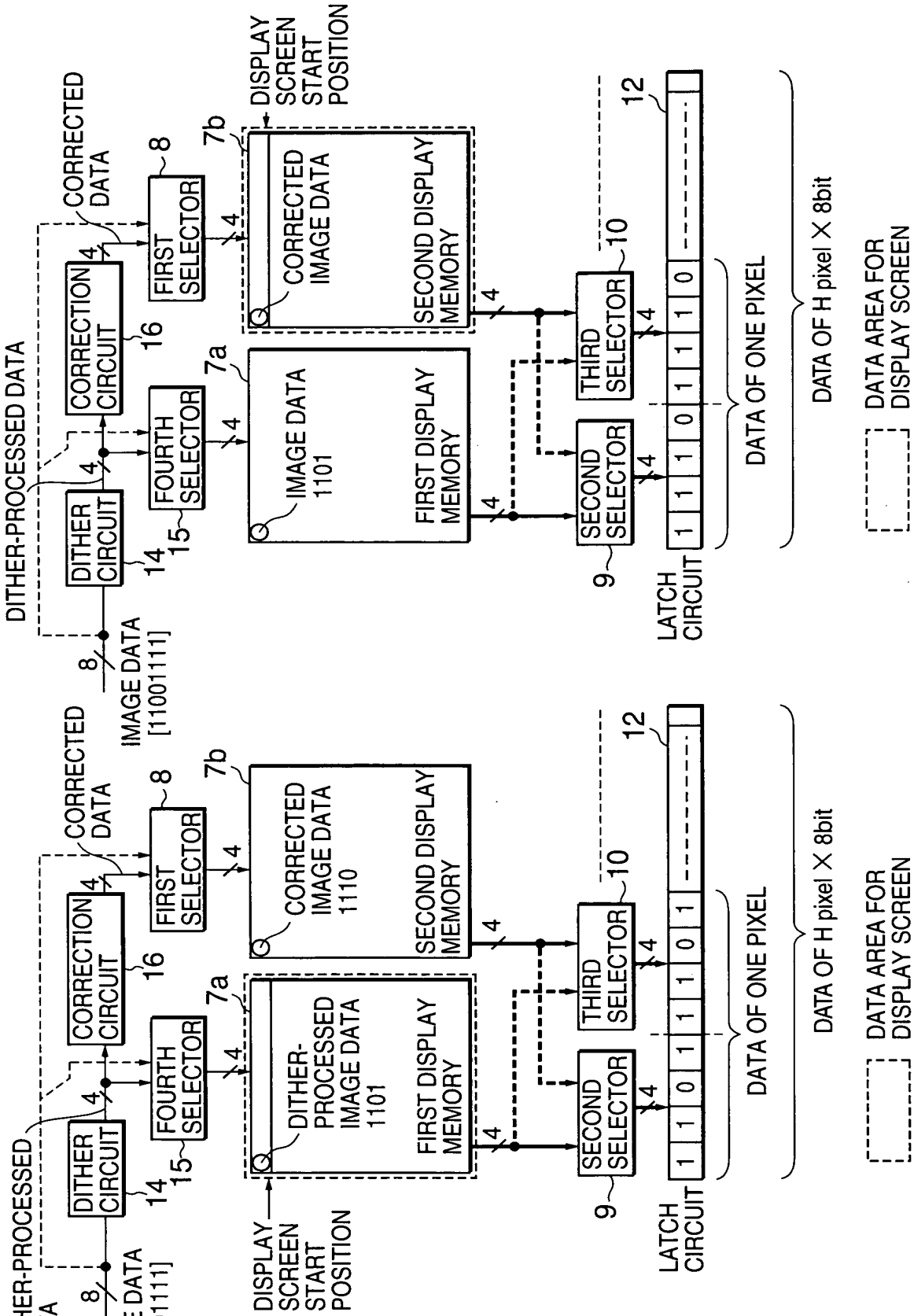

FIG. 18A

FIG. 18B

MEMORY PARTITION SIGNAL (SELECT 1)	MEMORY READ SELECT SIGNAL (SELECT 2)	FIRST OUTPUT SELECTOR	SECOND OUTPUT SELECTOR	THIRD OUTPUT SELECTOR	FOURTH OUTPUT SELECTOR
OFF	OFF	LOW ORDER 4 BITS OF IMAGE DATA	— —	— —	HIGH ORDER 4 BITS OF IMAGE DATA
OFF	ON	LOW ORDER 4 BITS OF IMAGE DATA	DATA STORED IN FIRST DISPLAY MEMORY	DATA STORED IN SECOND DISPLAY MEMORY	HIGH ORDER 4 BITS OF IMAGE DATA
ON	OFF	CORRECTED IMAGE DATA (HIGH ORDER 4 BITS)	DATA STORED IN FIRST DISPLAY MEMORY	DATA STORED IN FIRST DISPLAY MEMORY	DITHER-PROCESSED IMAGE DATA (HIGH ORDER 4 BITS)
ON	ON	CORRECTED IMAGE DATA (HIGH ORDER 4 BITS)	DATA STORED IN SECOND DISPLAY MEMORY	DATA STORED IN SECOND DISPLAY MEMORY	DITHER-PROCESSED IMAGE DATA (HIGH ORDER 4 BITS)

FIG. 19

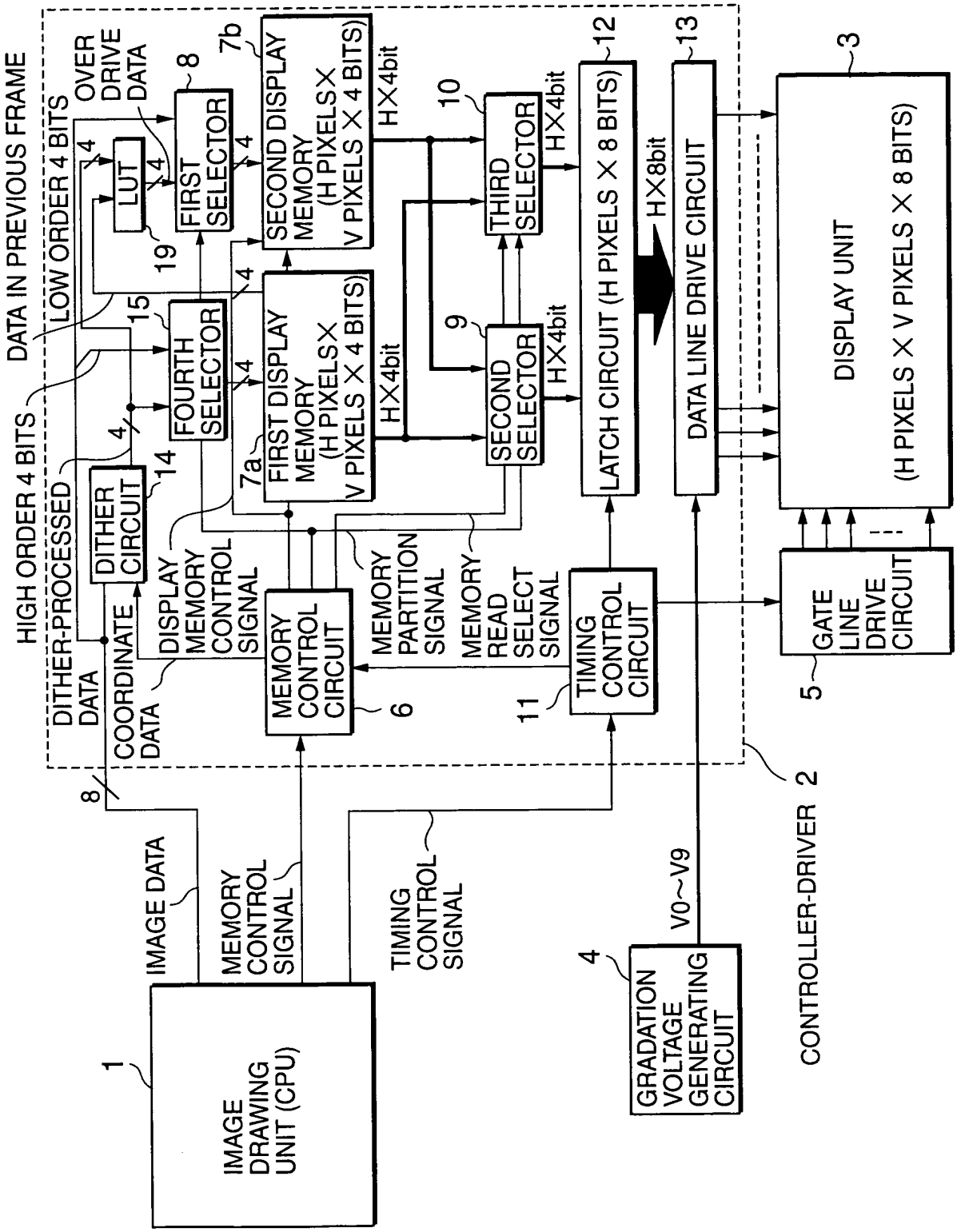
IMAGE DRAWING UNIT (CPU)
1
IMAGE DATA
MEMORY CONTROL SIGNAL
TIMING CONTROL SIGNAL
8
CONTROLLER-DRIVER 2
GRADATION VOLTAGE GENERATING CIRCUIT
4
V0~V9
GATE LINE DRIVE CIRCUIT
5
DISPLAY UNIT
(H PIXELS × V PIXELS × 8 BITS)
3
DATA LINE DRIVE CIRCUIT
HX8bit
LATCH CIRCUIT (H PIXELS × 8 BITS)
12
TIMING CONTROL CIRCUIT
11
MEMORY CONTROL CIRCUIT
6
MEMORY READ SELECT SIGNAL
MEMORY PARTITION SIGNAL
DISPLAY MEMORY CONTROL SIGNAL
COORDINATE DATA
DITHER-PROCESSED DATA
DITHER CIRCUIT
14
4
FOURTH SELECTOR
15
FIRST DISPLAY MEMORY (H PIXELS× V PIXELS × 4 BITS)
7a
HX4bit
SECOND SELECTOR
9
HX4bit
THIRD SELECTOR
10
HX4bit
SECOND DISPLAY MEMORY (H PIXELS× V PIXELS × 4 BITS)
7b
FIRST SELECTOR
8
LUT
19
HIGH ORDER 4 BITS
DATA IN PREVIOUS FRAME
LOW ORDER 4 BITS
OVER DRIVE DATA

FIG. 20

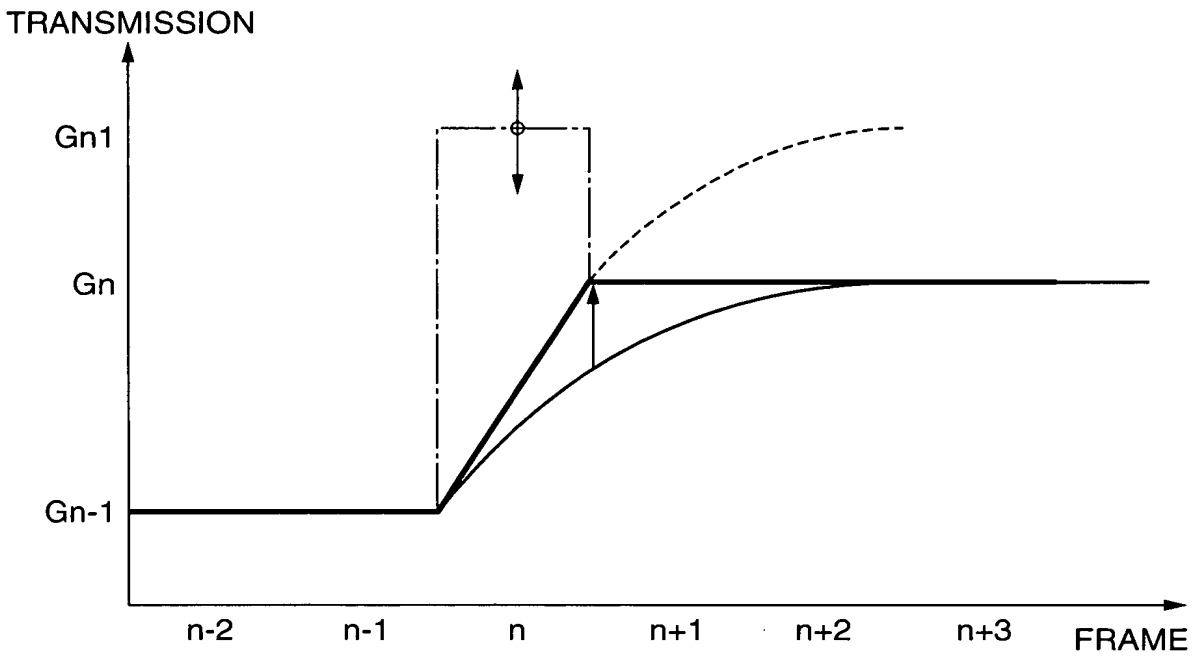

FIG. 21

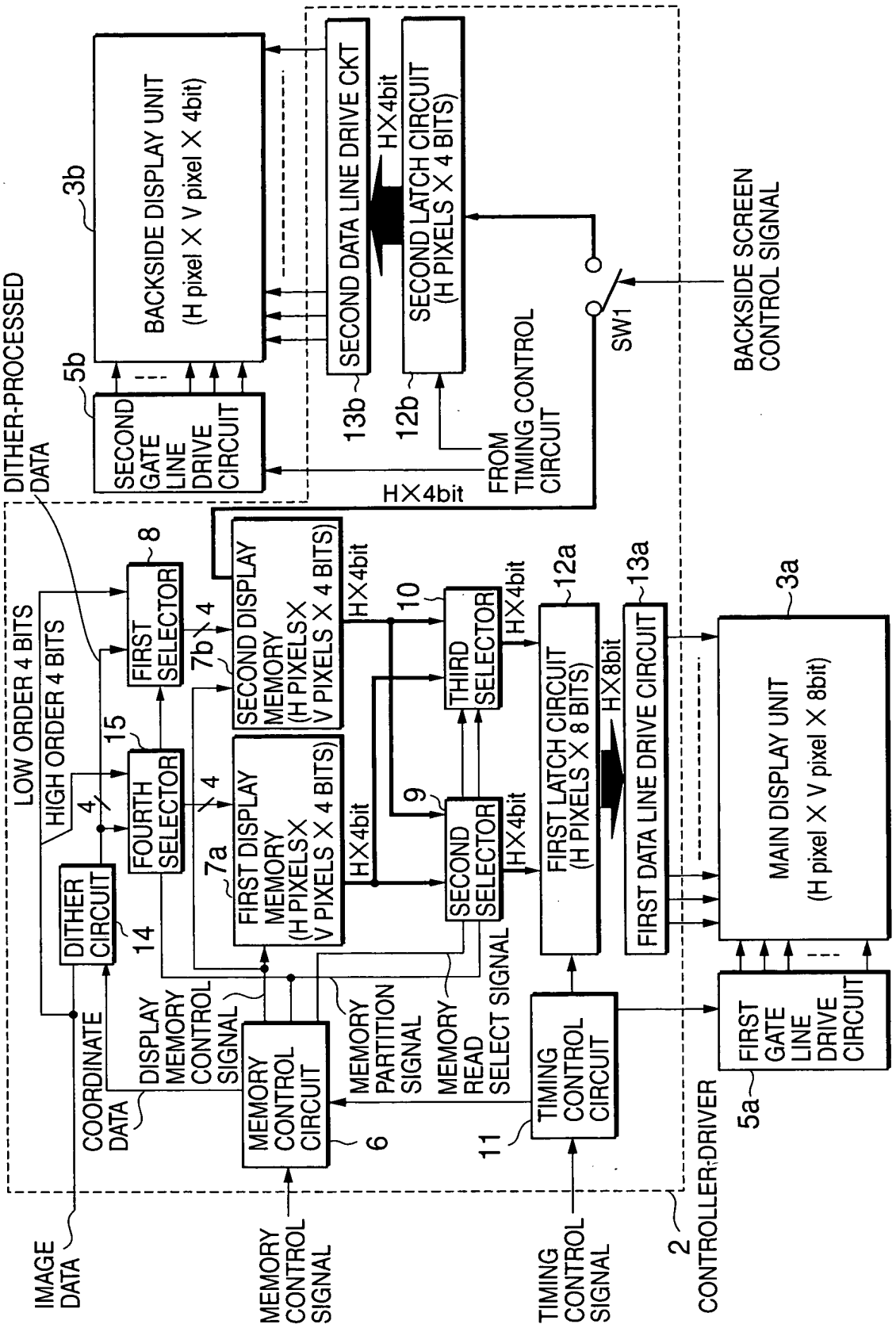
IMAGE DATA
MEMORY CONTROL SIGNAL
TIMING CONTROL SIGNAL
2 CONTROLLER-DRIVER
DITHER-PROCESSED DATA
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
DITHER CIRCUIT
14
FOURTH SELECTOR
15
FIRST SELECTOR
8
FIRST DISPLAY MEMORY (H PIXELS X V PIXELS X 4 BITS)
7a
SECOND DISPLAY MEMORY (H PIXELS X V PIXELS X 4 BITS)
7b
THIRD SELECTOR
10
SECOND SELECTOR
9
FIRST LATCH CIRCUIT (H PIXELS X 8 BITS)
12a
FIRST DATA LINE DRIVE CIRCUIT
13a
MAIN DISPLAY UNIT (H pixel X V pixel X 8bit)
3a
FIRST GATE LINE DRIVE CIRCUIT
5a
MEMORY CONTROL CIRCUIT
6
TIMING CONTROL CIRCUIT
11
COORDINATE DATA
DISPLAY MEMORY CONTROL SIGNAL
MEMORY PARTITION SIGNAL
MEMORY READ SELECT SIGNAL
HX4bit
HX8bit
SECOND GATE LINE DRIVE CIRCUIT
5b
BACKSIDE DISPLAY UNIT (H pixel X V pixel X 4bit)
3b
SECOND DATA LINE DRIVE CKT
13b
SECOND LATCH CIRCUIT (H PIXELS X 4 BITS)
12b
FROM TIMING CONTROL CIRCUIT
SW1
BACKSIDE SCREEN CONTROL SIGNAL

FIG. 22

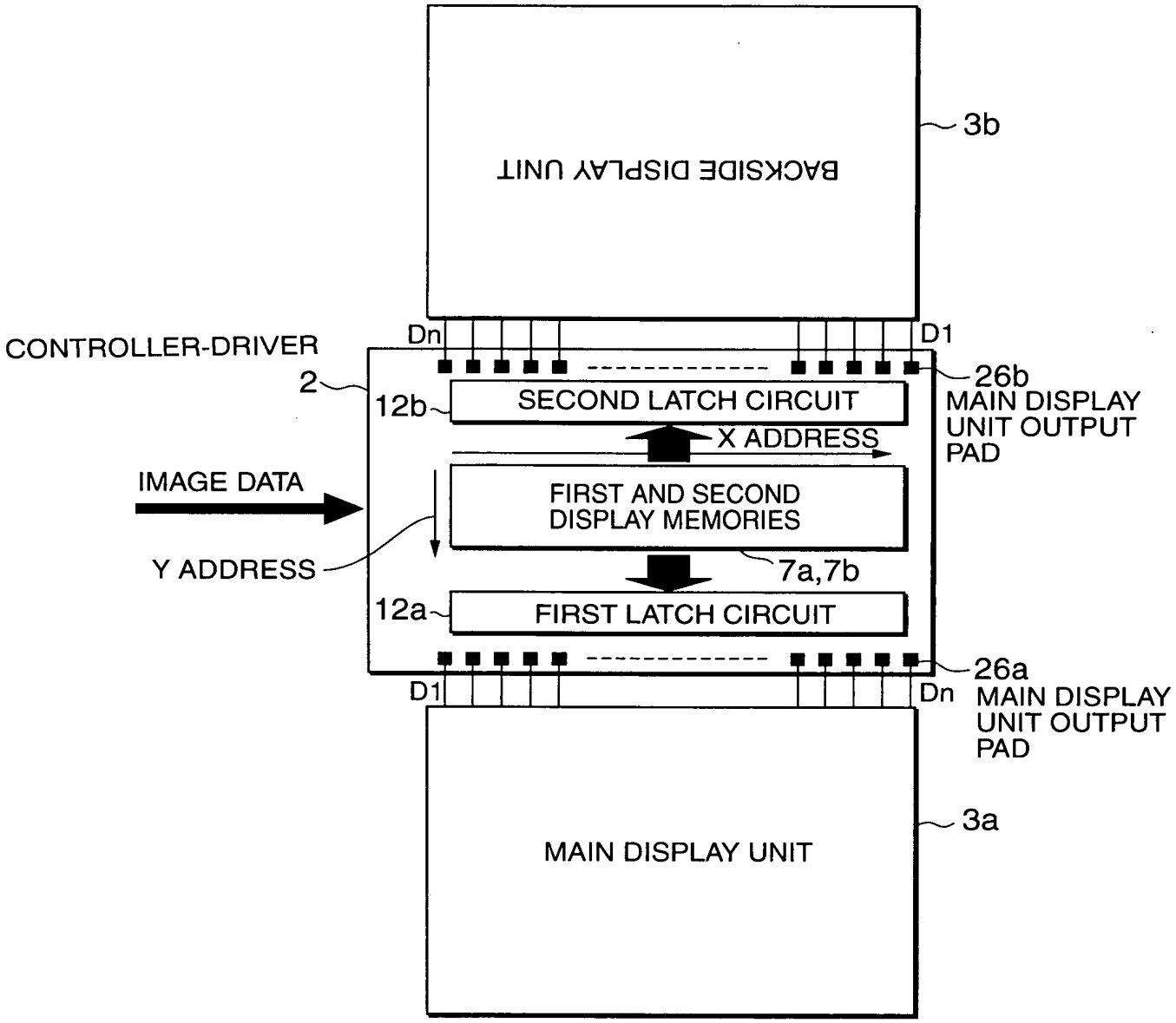
BACKSIDE DISPLAY UNIT
3b
CONTROLLER-DRIVER
2
Dn
D1
12b
SECOND LATCH CIRCUIT
26b
MAIN DISPLAY UNIT OUTPUT PAD
X ADDRESS
IMAGE DATA
FIRST AND SECOND DISPLAY MEMORIES
Y ADDRESS
7a,7b
12a
FIRST LATCH CIRCUIT
26a
MAIN DISPLAY UNIT OUTPUT PAD
D1
Dn
3a
MAIN DISPLAY UNIT

FIG. 23

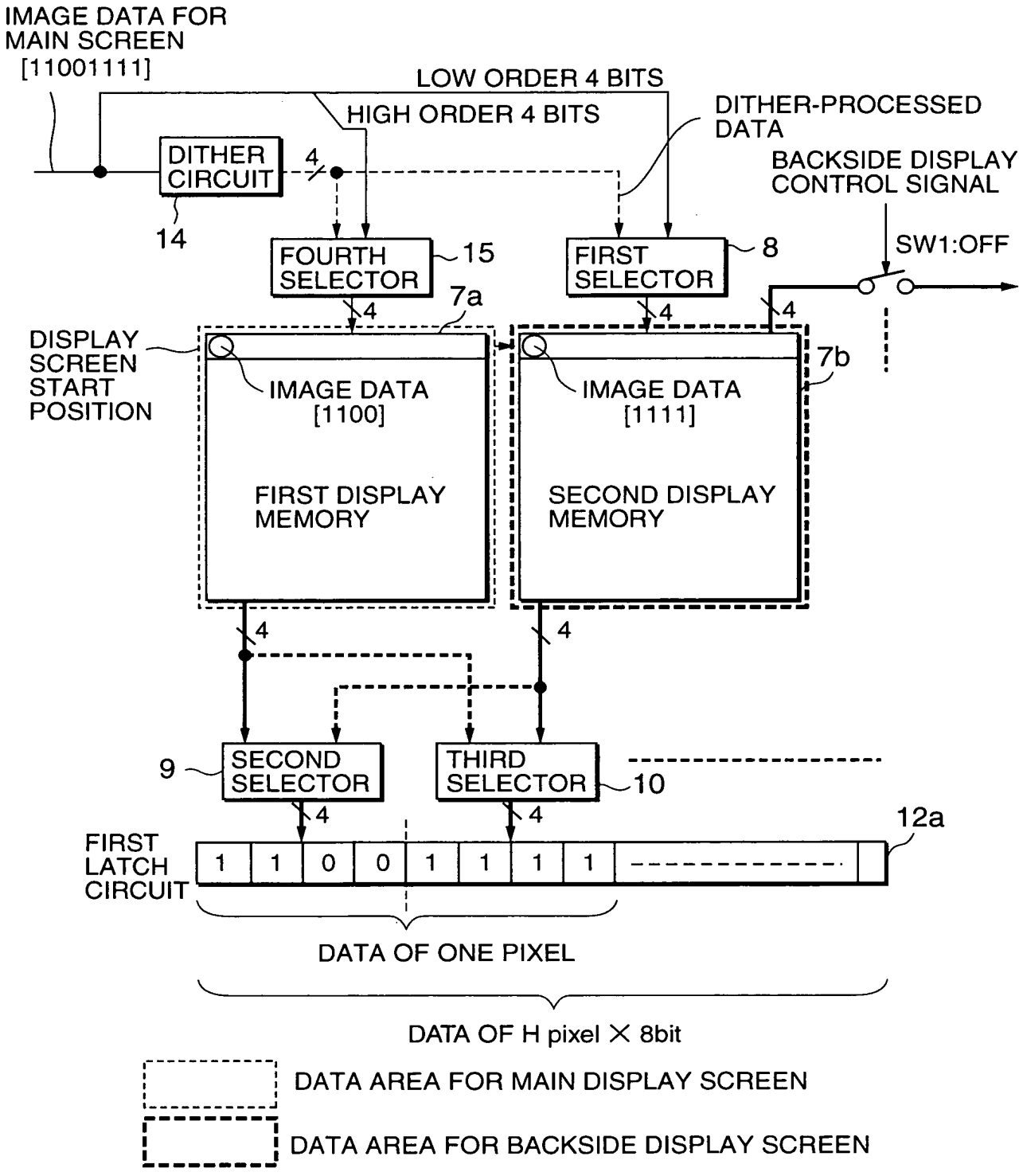
IMAGE DATA FOR MAIN SCREEN [11001111]
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
DITHER-PROCESSED DATA
BACKSIDE DISPLAY CONTROL SIGNAL
DITHER CIRCUIT
4
14
FOURTH SELECTOR
15
FIRST SELECTOR
8
SW1:OFF
7a
DISPLAY SCREEN START POSITION
IMAGE DATA [1100]
IMAGE DATA [1111]
7b
FIRST DISPLAY MEMORY
SECOND DISPLAY MEMORY
9
SECOND SELECTOR
THIRD SELECTOR
10
12a
FIRST LATCH CIRCUIT
1 1 0 0 1 1 1 1
DATA OF ONE PIXEL
DATA OF H pixel × 8bit
DATA AREA FOR MAIN DISPLAY SCREEN
DATA AREA FOR BACKSIDE DISPLAY SCREEN

FIG. 24

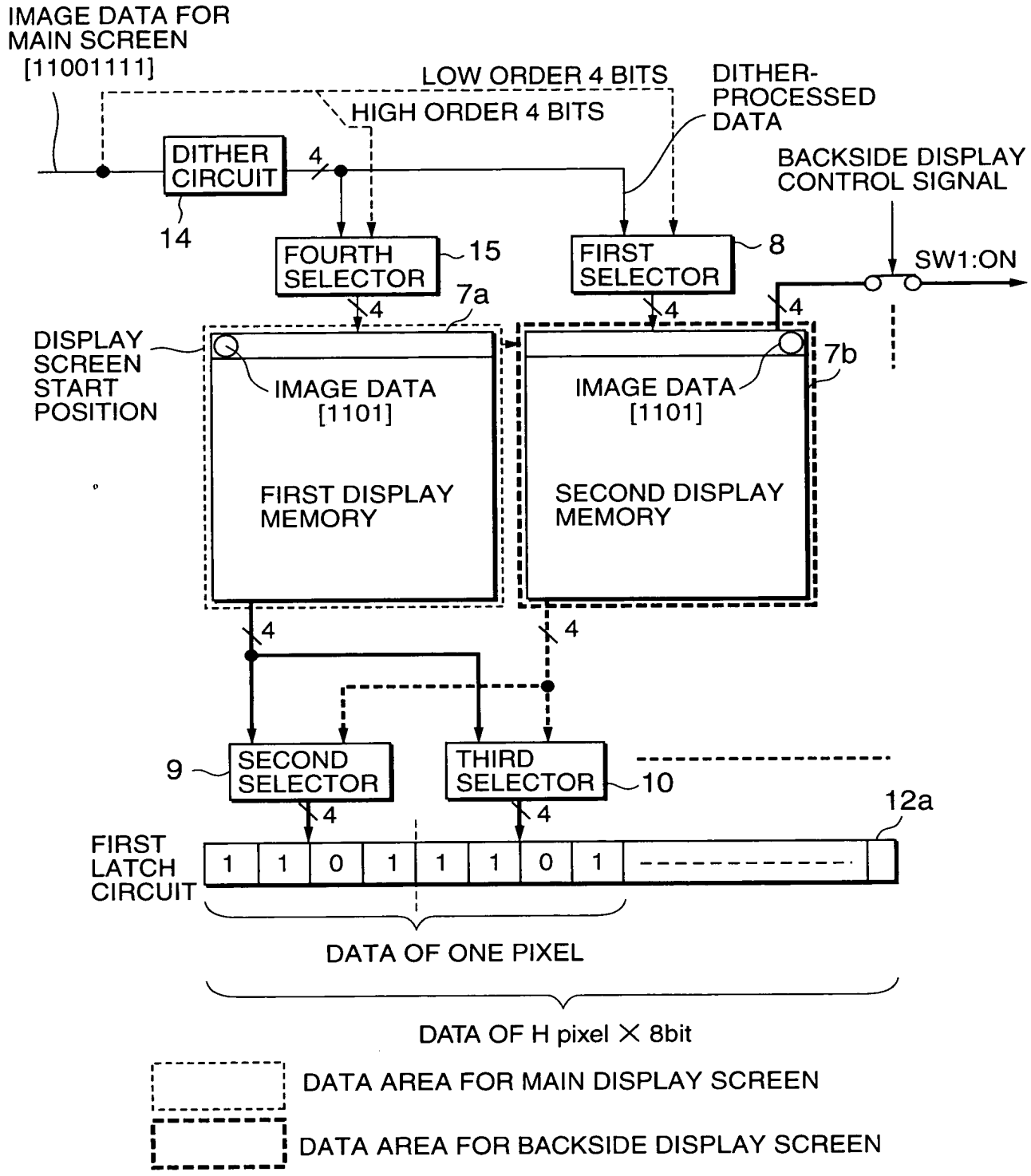
IMAGE DATA FOR MAIN SCREEN [11001111]
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
DITHER-PROCESSED DATA
DITHER CIRCUIT
4
14
BACKSIDE DISPLAY CONTROL SIGNAL
SW1:ON
FOURTH SELECTOR
15
FIRST SELECTOR
8
7a
7b
DISPLAY SCREEN START POSITION
IMAGE DATA [1101]
IMAGE DATA [1101]
FIRST DISPLAY MEMORY
SECOND DISPLAY MEMORY
9
SECOND SELECTOR
THIRD SELECTOR
10
12a
FIRST LATCH CIRCUIT
1 1 0 1 1 1 0 1
DATA OF ONE PIXEL
DATA OF H pixel × 8bit
DATA AREA FOR MAIN DISPLAY SCREEN
DATA AREA FOR BACKSIDE DISPLAY SCREEN

FIG. 25

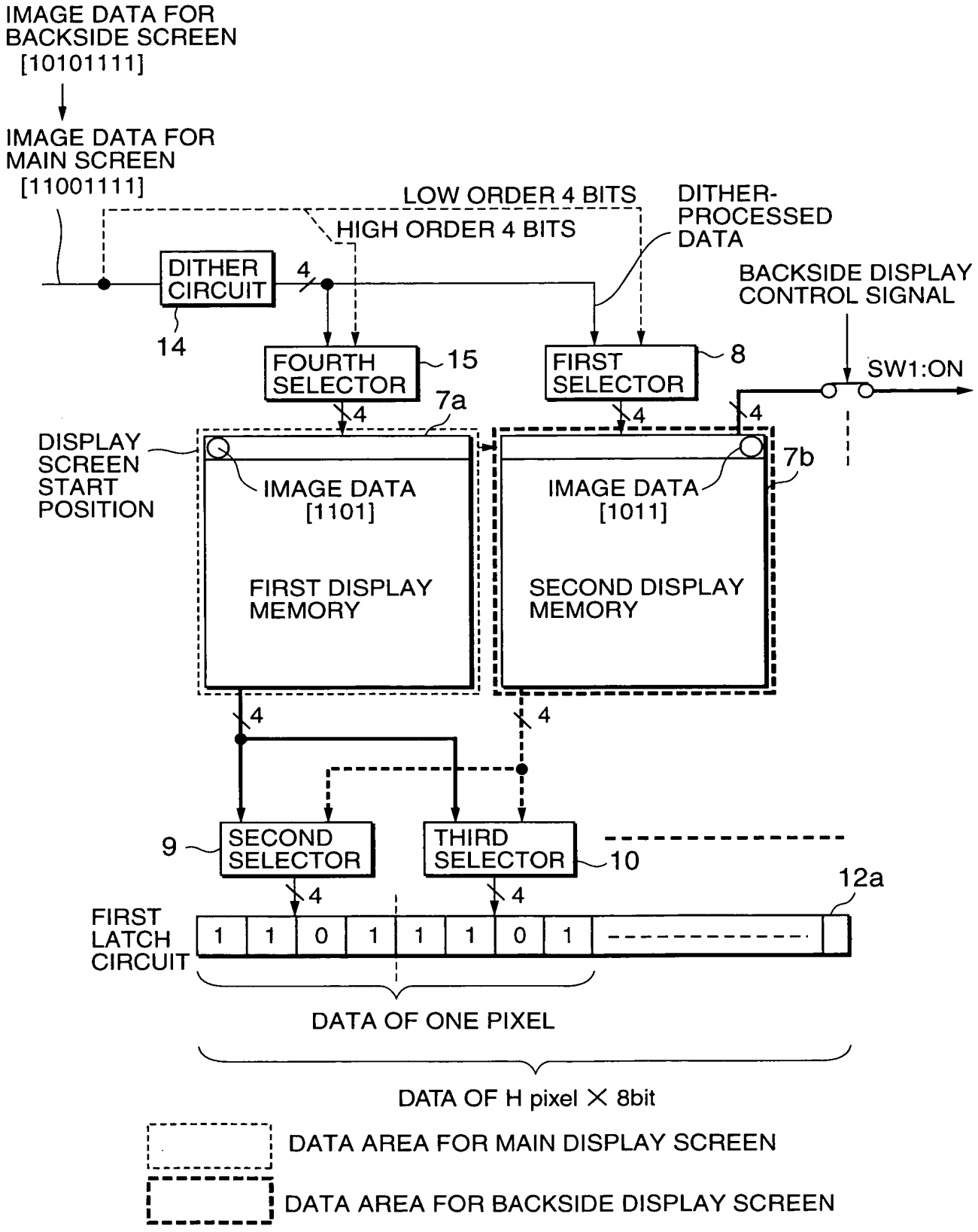
IMAGE DATA FOR BACKSIDE SCREEN
[10101111]
IMAGE DATA FOR MAIN SCREEN
[11001111]
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
DITHER-PROCESSED DATA
DITHER CIRCUIT
4
14
BACKSIDE DISPLAY CONTROL SIGNAL
SW1:ON
FOURTH SELECTOR
15
FIRST SELECTOR
8
7a
DISPLAY SCREEN START POSITION
IMAGE DATA [1101]
IMAGE DATA [1011]
7b
FIRST DISPLAY MEMORY
SECOND DISPLAY MEMORY
9
SECOND SELECTOR
THIRD SELECTOR
10
12a
FIRST LATCH CIRCUIT
1 1 0 1 1 1 0 1
DATA OF ONE PIXEL
DATA OF H pixel × 8bit
DATA AREA FOR MAIN DISPLAY SCREEN
DATA AREA FOR BACKSIDE DISPLAY SCREEN

FIG. 26

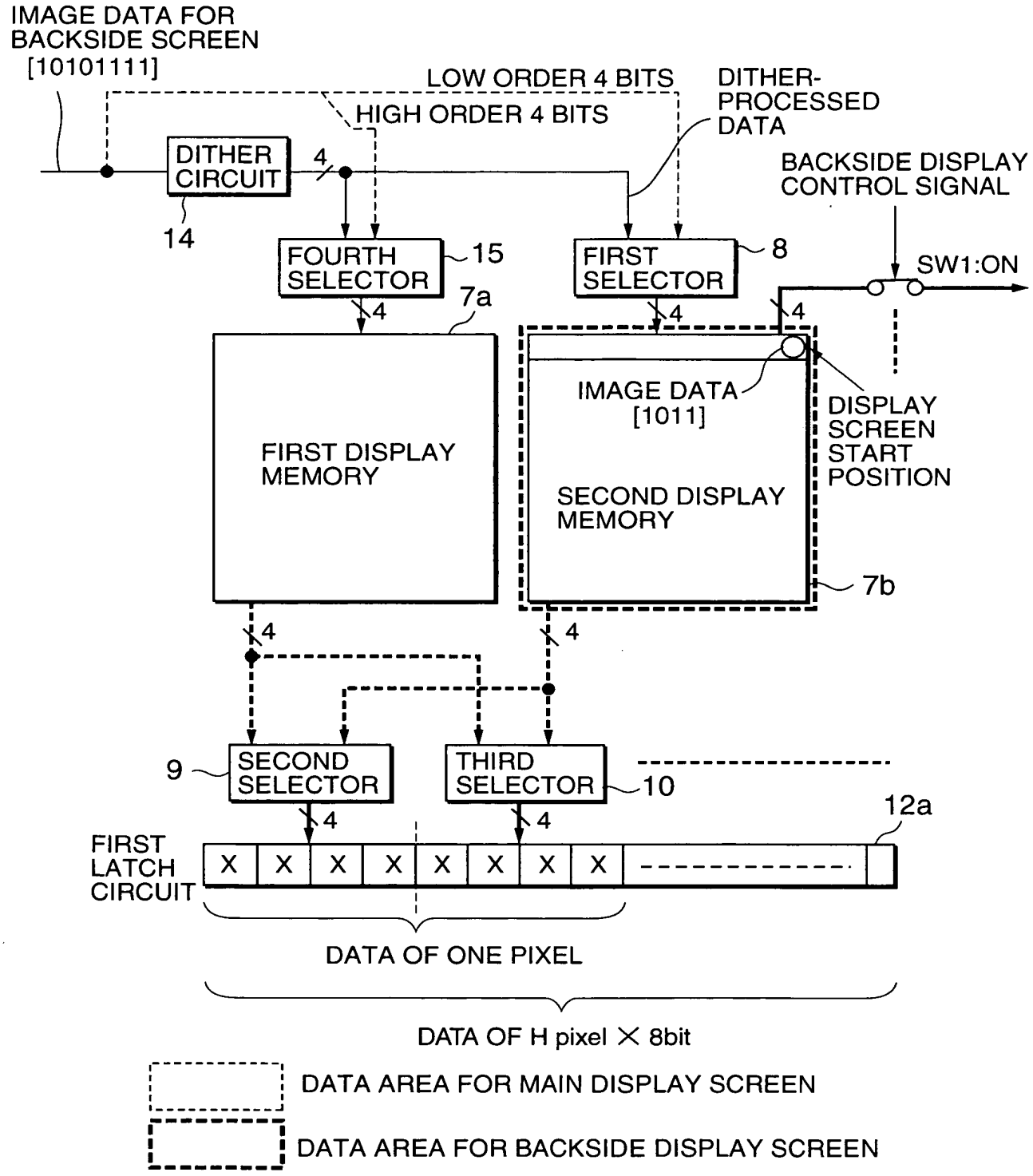
IMAGE DATA FOR BACKSIDE SCREEN
[10101111]
LOW ORDER 4 BITS
HIGH ORDER 4 BITS
DITHER-PROCESSED DATA
DITHER CIRCUIT
4
14
BACKSIDE DISPLAY CONTROL SIGNAL
SW1:ON
FOURTH SELECTOR
15
FIRST SELECTOR
8
7a
IMAGE DATA [1011]
DISPLAY SCREEN START POSITION
FIRST DISPLAY MEMORY
SECOND DISPLAY MEMORY
7b
9
SECOND SELECTOR
THIRD SELECTOR
10
12a
FIRST LATCH CIRCUIT
X X X X X X X X
DATA OF ONE PIXEL
DATA OF H pixel × 8bit
DATA AREA FOR MAIN DISPLAY SCREEN
DATA AREA FOR BACKSIDE DISPLAY SCREEN

FIG. 27

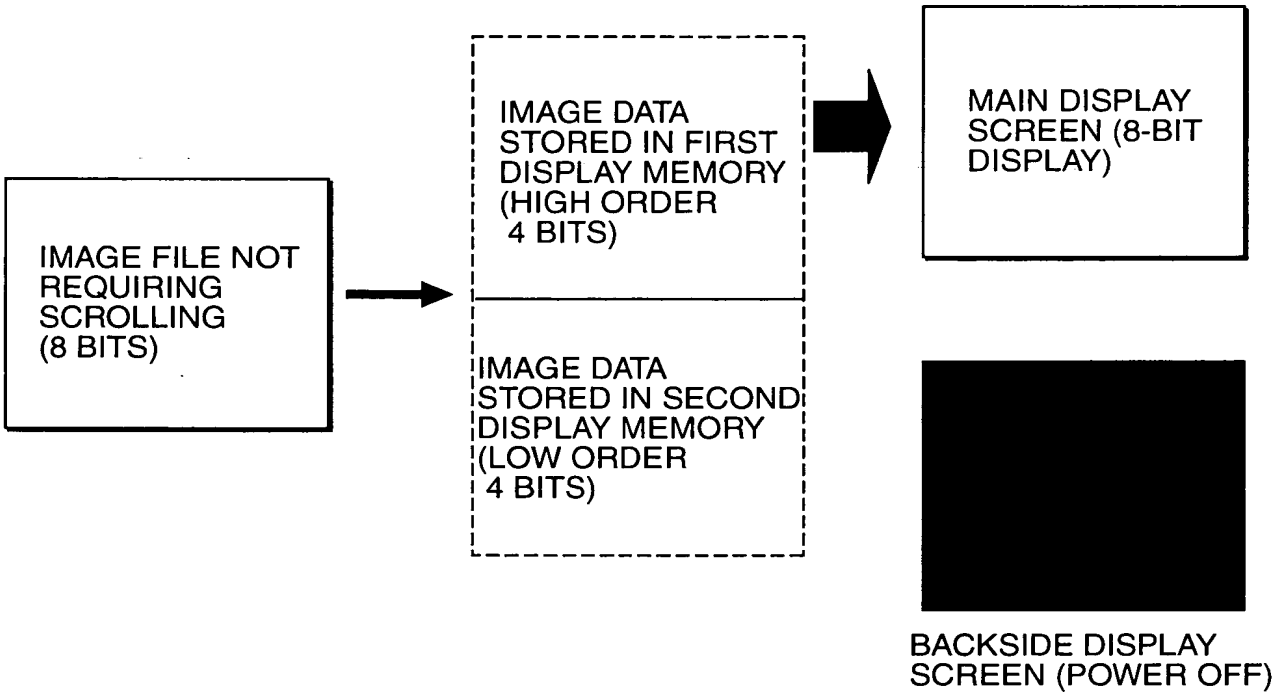
IMAGE FILE NOT REQUIRING SCROLLING (8 BITS)
IMAGE DATA STORED IN FIRST DISPLAY MEMORY (HIGH ORDER 4 BITS)
IMAGE DATA STORED IN SECOND DISPLAY MEMORY (LOW ORDER 4 BITS)
MAIN DISPLAY SCREEN (8-BIT DISPLAY)
BACKSIDE DISPLAY SCREEN (POWER OFF)

FIG. 28

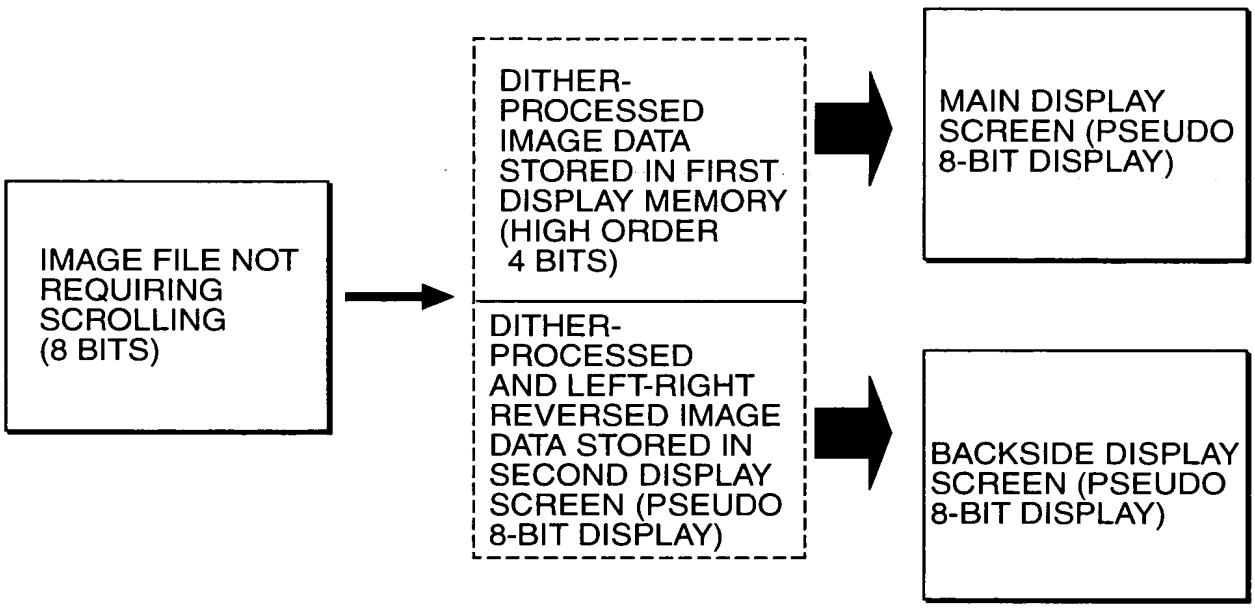
IMAGE FILE NOT REQUIRING SCROLLING (8 BITS)
DITHER-PROCESSED IMAGE DATA STORED IN FIRST DISPLAY MEMORY (HIGH ORDER 4 BITS)
DITHER-PROCESSED AND LEFT-RIGHT REVERSED IMAGE DATA STORED IN SECOND DISPLAY SCREEN (PSEUDO 8-BIT DISPLAY)
MAIN DISPLAY SCREEN (PSEUDO 8-BIT DISPLAY)
BACKSIDE DISPLAY SCREEN (PSEUDO 8-BIT DISPLAY)

FIG. 29

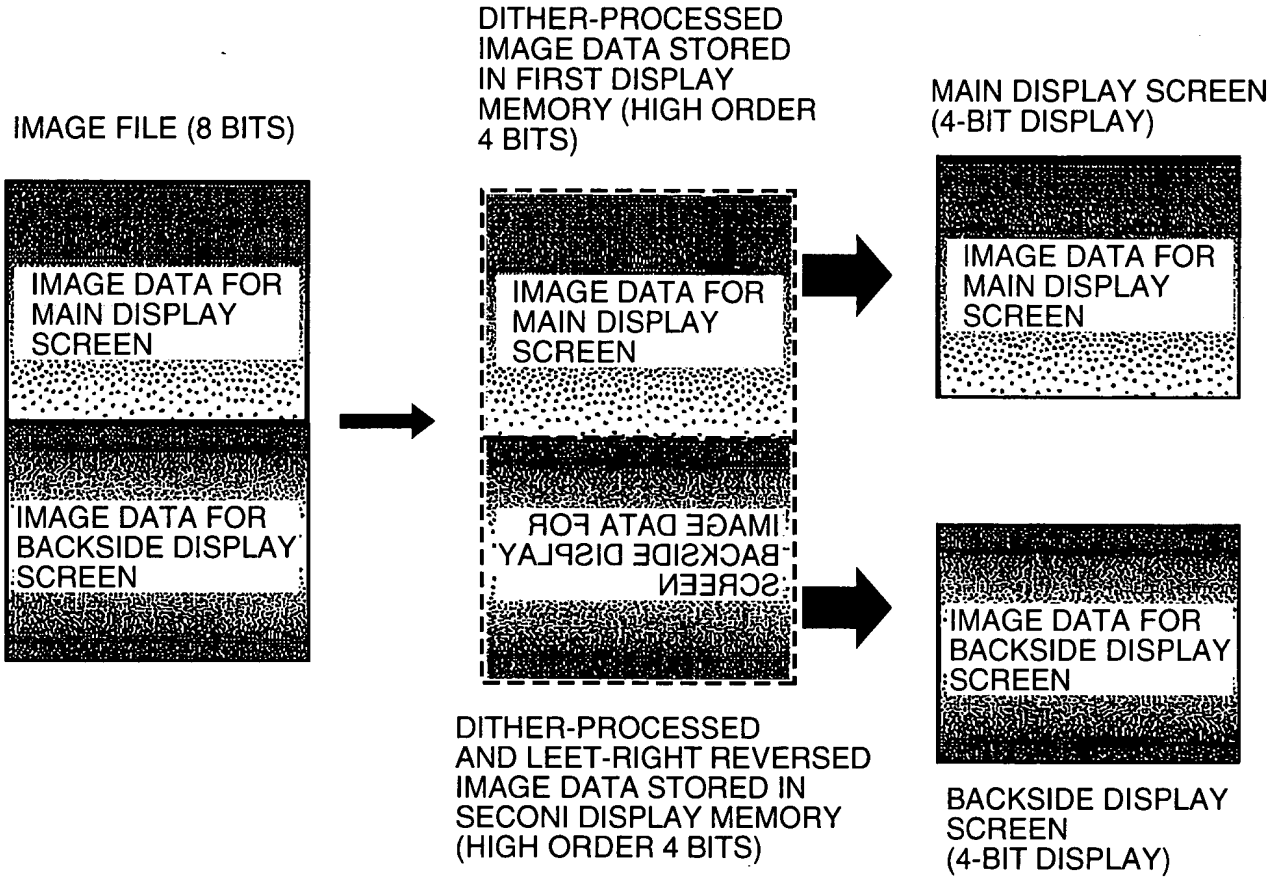
IMAGE FILE (8 BITS)
IMAGE DATA FOR MAIN DISPLAY SCREEN
IMAGE DATA FOR BACKSIDE DISPLAY SCREEN
DITHER-PROCESSED IMAGE DATA STORED IN FIRST DISPLAY MEMORY (HIGH ORDER 4 BITS)
IMAGE DATA FOR MAIN DISPLAY SCREEN
IMAGE DATA FOR BACKSIDE DISPLAY SCREEN
DITHER-PROCESSED AND LEET-RIGHT REVERSED IMAGE DATA STORED IN SECONI DISPLAY MEMORY (HIGH ORDER 4 BITS)
MAIN DISPLAY SCREEN (4-BIT DISPLAY)
IMAGE DATA FOR MAIN DISPLAY SCREEN
IMAGE DATA FOR BACKSIDE DISPLAY SCREEN
BACKSIDE DISPLAY SCREEN (4-BIT DISPLAY)

FIG. 30

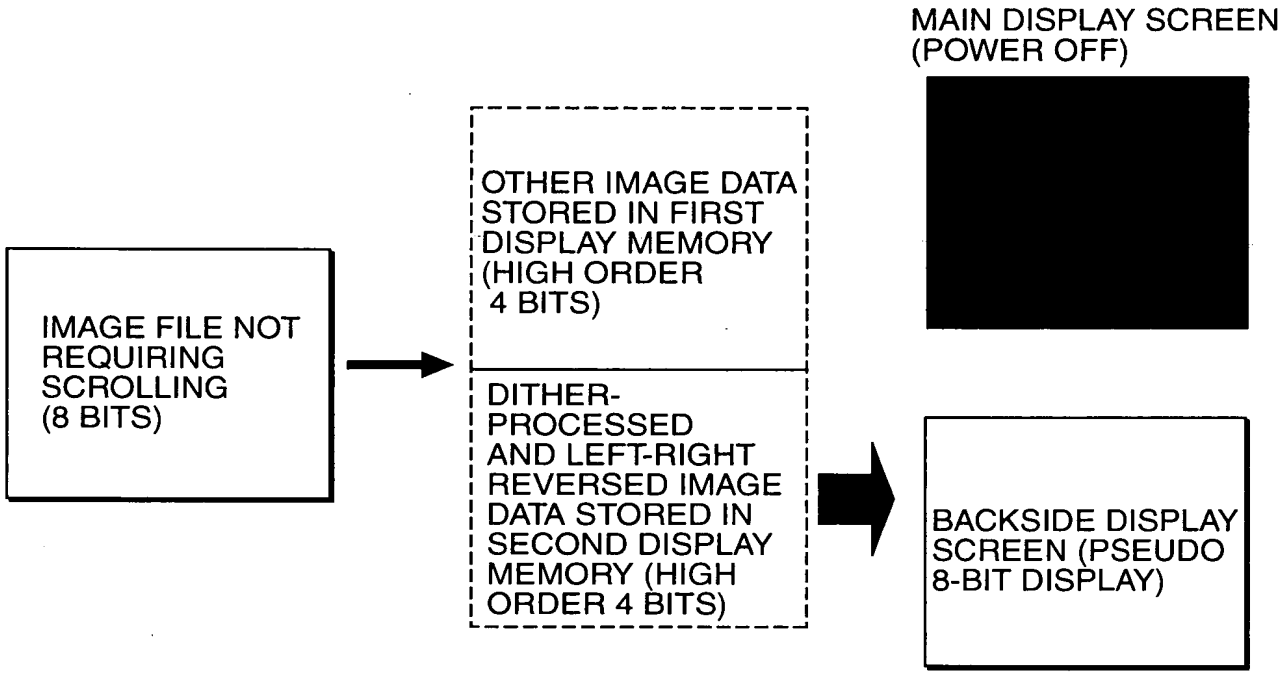
MAIN DISPLAY SCREEN (POWER OFF)
IMAGE FILE NOT REQUIRING SCROLLING (8 BITS)
OTHER IMAGE DATA STORED IN FIRST DISPLAY MEMORY (HIGH ORDER 4 BITS)
DITHER-PROCESSED AND LEFT-RIGHT REVERSED IMAGE DATA STORED IN SECOND DISPLAY MEMORY (HIGH ORDER 4 BITS)
BACKSIDE DISPLAY SCREEN (PSEUDO 8-BIT DISPLAY)

FIG. 31

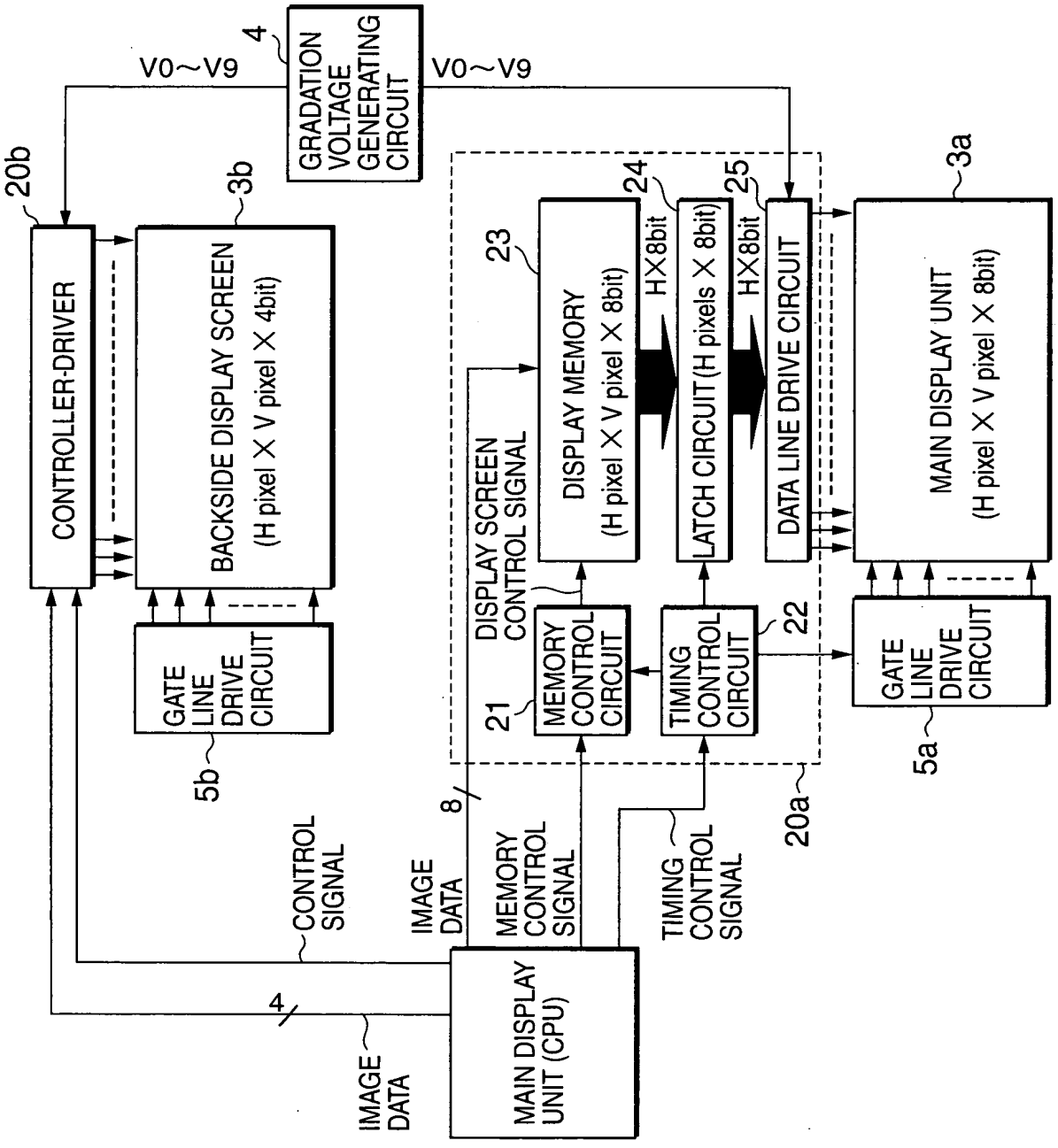
GRADATION VOLTAGE GENERATING CIRCUIT
4
V0~V9
V0~V9
20b
CONTROLLER-DRIVER
3b
BACKSIDE DISPLAY SCREEN
(H pixel X V pixel X 4bit)
GATE LINE DRIVE CIRCUIT
5b
23
DISPLAY MEMORY
(H pixel X V pixel X 8bit)
24
HX8bit
LATCH CIRCUIT (H pixels X 8bit)
25
HX8bit
DATA LINE DRIVE CIRCUIT
3a
MAIN DISPLAY UNIT
(H pixel X V pixel X 8bit)
DISPLAY SCREEN CONTROL SIGNAL
21
MEMORY CONTROL CIRCUIT
TIMING CONTROL CIRCUIT
22
GATE LINE DRIVE CIRCUIT
5a
20a
8
IMAGE DATA
MEMORY CONTROL SIGNAL
TIMING CONTROL SIGNAL
CONTROL SIGNAL
4
IMAGE DATA
MAIN DISPLAY UNIT (CPU)

FIG. 32

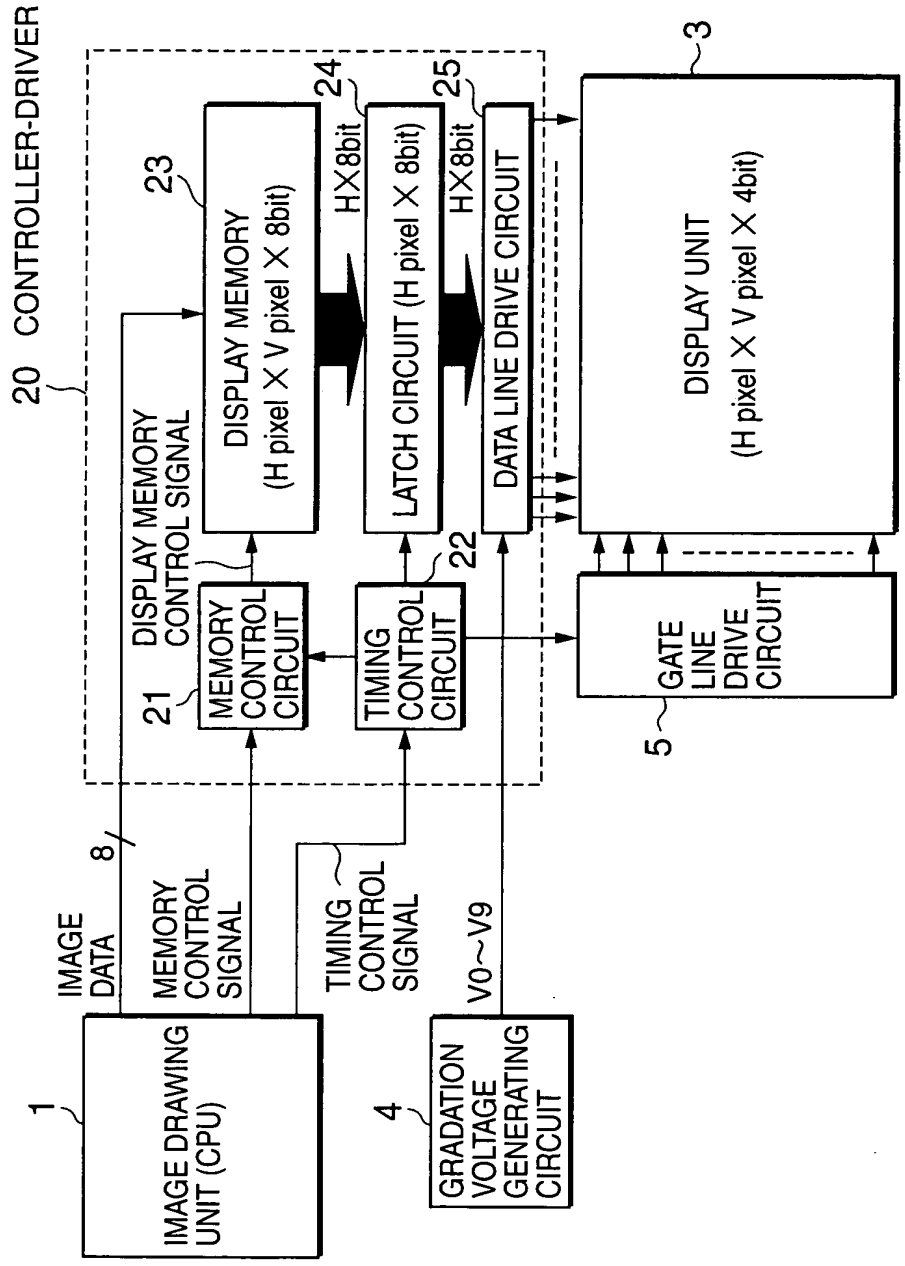
20 CONTROLLER-DRIVER
23
DISPLAY MEMORY
(H pixel X V pixel X 8bit)
24
HX8bit
25
LATCH CIRCUIT (H pixel X 8bit)
HX8bit
DATA LINE DRIVE CIRCUIT
3
DISPLAY UNIT
(H pixel X V pixel X 4bit)
DISPLAY MEMORY CONTROL SIGNAL
21
MEMORY CONTROL CIRCUIT
22
TIMING CONTROL CIRCUIT
GATE LINE DRIVE CIRCUIT
5
8
IMAGE DATA
MEMORY CONTROL SIGNAL
TIMING CONTROL SIGNAL
V0~V9
1
IMAGE DRAWING UNIT (CPU)
4
GRADATION VOLTAGE GENERATING CIRCUIT

FIG. 33